# 3 kW dual-phase LLC demo board

## Using 600 V CoolMOS™ CDF7 and digital control by XMC4400

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## About this document

### Scope and purpose

This document describes the design and performance of a 3 kW dual-phase LLC evaluation board intended for use in the isolated HV DC-DC stage of an SMPS for telecom and industrial applications.

This is a high-performance example with a complete Infineon solution, including HV and LV power MOSFETs, controllers and drivers, demonstrating a very effective way to design the HV DC-DC stage of a telecom rectifier or industrial SMPS that meets the highest standards of efficiency and reliability. The additional benefit of a very flat efficiency plot is also achieved through a mix of proper control techniques and best-in-class power device selection.

Key Infineon products used to achieve this performance level include:

- 600 V CoolMOS™ CFD7 SJ MOSFET
- Isolated gate drive 1EDI60N12AF
- SR MOSFETs OptiMOS™ BSC093N15NS5
- Advanced dual-channel gate drive 2EDN7524
- XMC4400 microcontroller
- Bias QR Flyback controller ICE2QR2280Z

As well as design information and documentation for the LLC converter, the reader will receive additional information on how the 600 V CoolMOS™ CFD7 behaves in LLC applications and the associated benefits, how the high-performance magnetics design can be approached, and insights into how to develop dual-phase LLC converters in similar power ranges adapted to specific requirements.

### Intended audience

This document is intended for design engineers who wish to evaluate high-performance topologies for High-Power (HP) SMPS converters, and develop an understanding of the design process and how to apply the multi-phase LLC design methods to their own system applications.

*Note: General knowledge about the resonant Half-Bridge (HB) LLC converter principle of operation is required for proper comprehension of the concepts reported in this paper.*

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# 1 Introduction

The combined trends of continuous reduction of volume and size of the power converters and increase of required output power represent a serious challenge in modern SMPS designs.

When addressing the HP density requirement, even in an SMPS with high peak efficiency, a typical problem is getting rid of the heat generated, especially at the full load, in the limited volume available.

A very powerful fan can help, but there may be a lot of side-effects, such as acoustic noise or vibration, which may be not tolerated by other system components, for example hard disk drives in computing applications. And in any case the effectiveness of the forced ventilation is linked to the air impedance inside the SMPS. Unfortunately, a typical consequence of the power density increase is the increase of the air impedance inside the PSU.

Especially in industrial and telecom applications, there are cases where the fan is even not allowed.

The best solution is to try to limit the heat generated, especially under the most critical conditions from the thermal perspective: full-load operation. This means that having a very high peak efficiency (typically achieved at 50% load) may not be enough for the purpose, but the same high efficiency has to be extended up to full-load operation.

In other words, this requirement involves the need for a very flat efficiency plot, at least from 40–50% up to 100% load.

On the other hand, in N + 1 redundant application the percentage of SMPS operation near full load is lower than that below half-load, also making efficiency down to around 30% load important.

The combination of these typical performance requirements of industrial and telecom HP SMPS can be fulfilled through a very flat efficiency plot, from 30% to 100% load.

A similar curve is not compatible with the natural behavior of a power converter, whose efficiency plot is typically a parabola, with the peak at around mid-load. In other words, the desired “flatness” can be achieved only through a dedicated power converter design, which involves proper selection of topologies, power devices, magnetic components and control techniques.

One of the most popular solutions adopted in power conversion in order to achieve this goal is the multi-phase approach. Scaling and balancing are two typical aspects of this design technique [15].

In this document the fundamental aspects of a Multi-phase LLC converter are analyzed, giving an overview of the most important design choices, especially in power semiconductors and control techniques.

A practical example is provided thorugh the description of a 3 kW dual-phase LLC demo board designed entirely with Infineon power semiconductors and IC components.

This document shows the use of state-of-the-art HV and MV silicon MOSFETs, combined with optimized driving and sophisticated digital control to meet the most important requirements of a modern HP SMPS, both in terms of performance and reliability.

With the goal of achieving high reliability in the design, a prominent role is played in the analyzed topology by the HV MOSFET used in each HB LLC Converter. The selection of CoolMOS™ CFD7 provides all the benefits of the latest generation of fast Body Diode (BD) devices, able to guarantee reliable operation even in the critical operating modes of the multi-phase LLC topology.

All the features of the CoolMOS™ CFD7 technology are described in detail in [17], which complements this AN.

# 2 Dual-phase HB LLC design concept

This AN provides a general overview of the Infineon 3 kW dual-phase LLC demo board and the concept behind it. Three important aspects of the present design are explained in this section. The specific control techniques used to address these three aspects will be explained in more detail in Section 4.

## 2.1 Current sharing and phase shedding

### 2.1.1 The design challenges

The principle of operation of a single HB LLC converter is described in detail in [1].

Unlike a conventional PWM topology, based on a fixed frequency and variable duty cycle control, a resonant converter uses the switching frequency ($F_{sw}$) as the main control parameter. The typical high gain of the resonant tank makes the resonant current ($I_{res}$) very sensitive to the operating frequency.

When two resonant converters operate in parallel at the same frequency, any mis-match between the components of the two resonant tanks can generate a current imbalance in the two converters, which in the worst case can force all the current into one of the two phases, thus generating over-stress and most likely shut-down due to the Over Current Protection (OCP) mechanism.

A simulation performed with Simetrix on a dual-phase LLC circuit (Figure 1) clearly demonstrates the design challenges related to the current-sharing implementation.

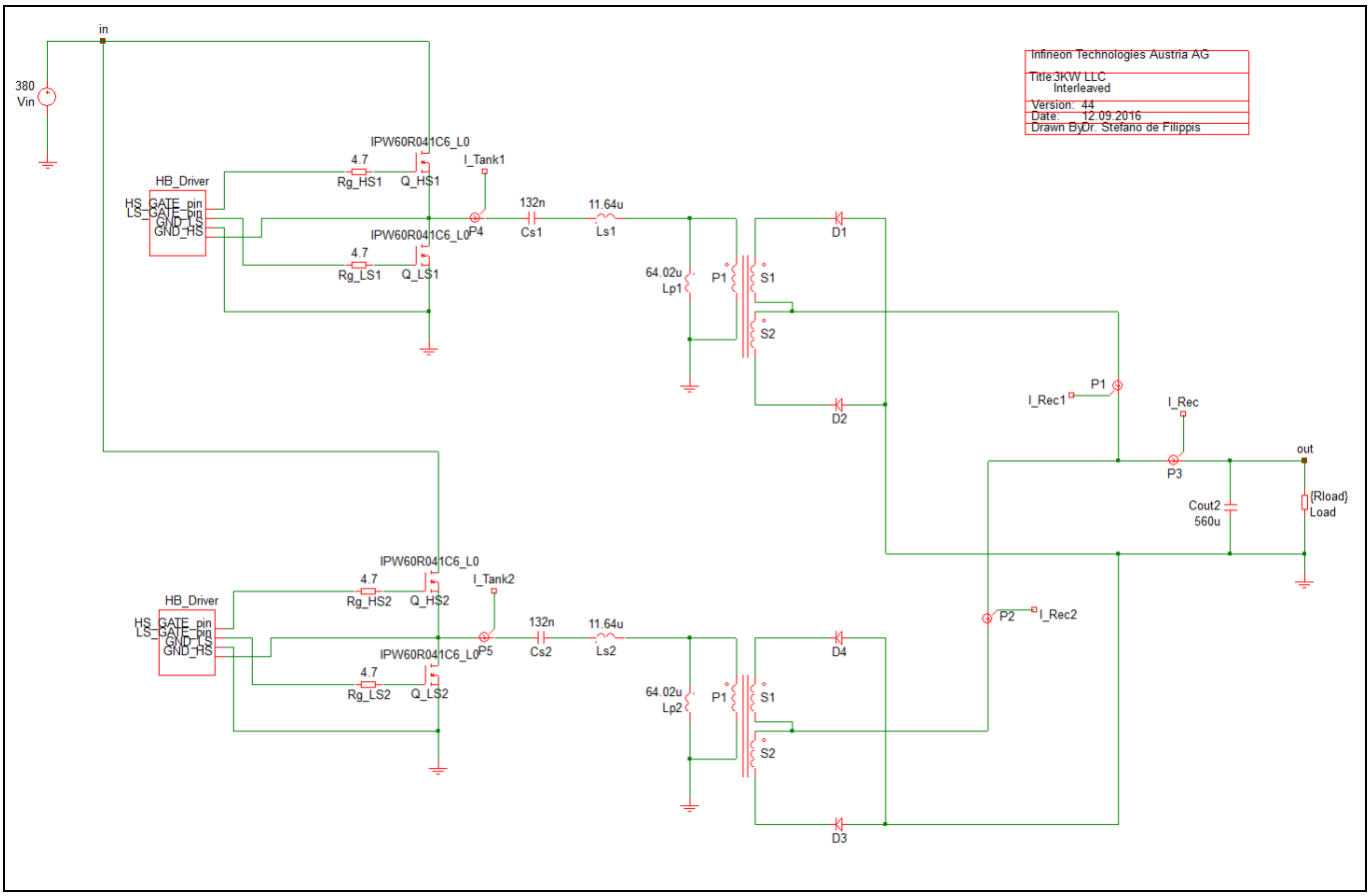



**Figure 1 Simetrix simulation model of the 3 kW dual-phase LLC**

### Dual-phase HB LLC design concept

Figures 2 and 3 (below) show the perfect balance of current in the two LLC converters, called Conv1 and Conv2 respectively, on both the primary and secondary side, in case of identical resonant tank components. The $F_{sw}$ used for the simulations is the resonant frequency, which is the same for both converters. All the waveforms (both primary and secondary) related to Conv1 are plotted in red; the ones related to Conv2 are plotted in green.

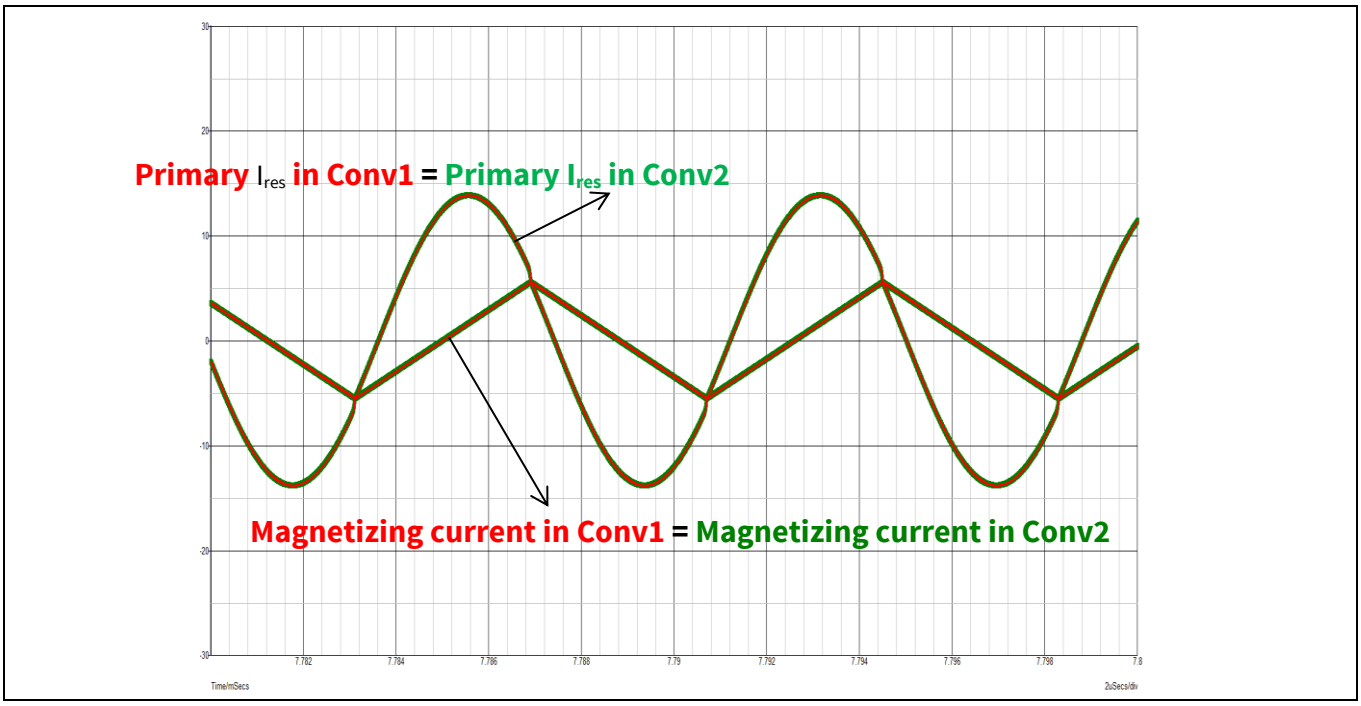



**Figure 2 Resonant and magnetizing currents in case of identical resonant tank components**

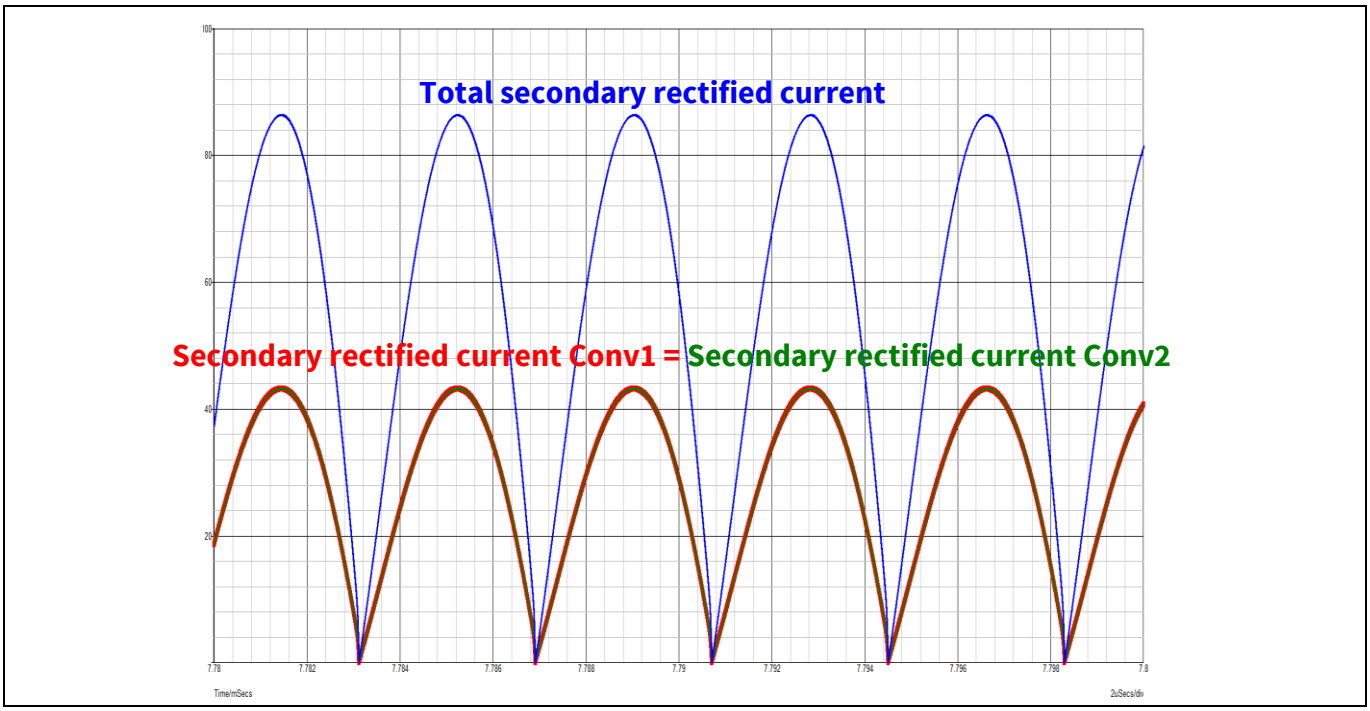



**Figure 3 Secondary rectified currents in case of identical resonant tank components**

From Figure 2 you can see that the primary resonant currents and, of course, the magnetizing currents are completely overlapping, as an obvious consequence of the perfect balance of the two phases, which should operate at the same resonant frequency. Figure 3 also shows that the secondary rectified currents are overlapping, and that each of them contributes by 50% to the full secondary rectified current, represented by the blue plot.

Figures 4, 5 and 6 refer to the case where there is a difference of only 5% between the values of the inductances in the two resonant tanks. Specifically, the resonant inductance ($L_r$) in the Conv2 ($L_{r2}$) is 5% smaller than the one in the other tank ($L_{r1}$). This is a very common situation in practice, due to the typical tolerances in the range of ±10% of the nominal values shown by this kind of magnetic component.

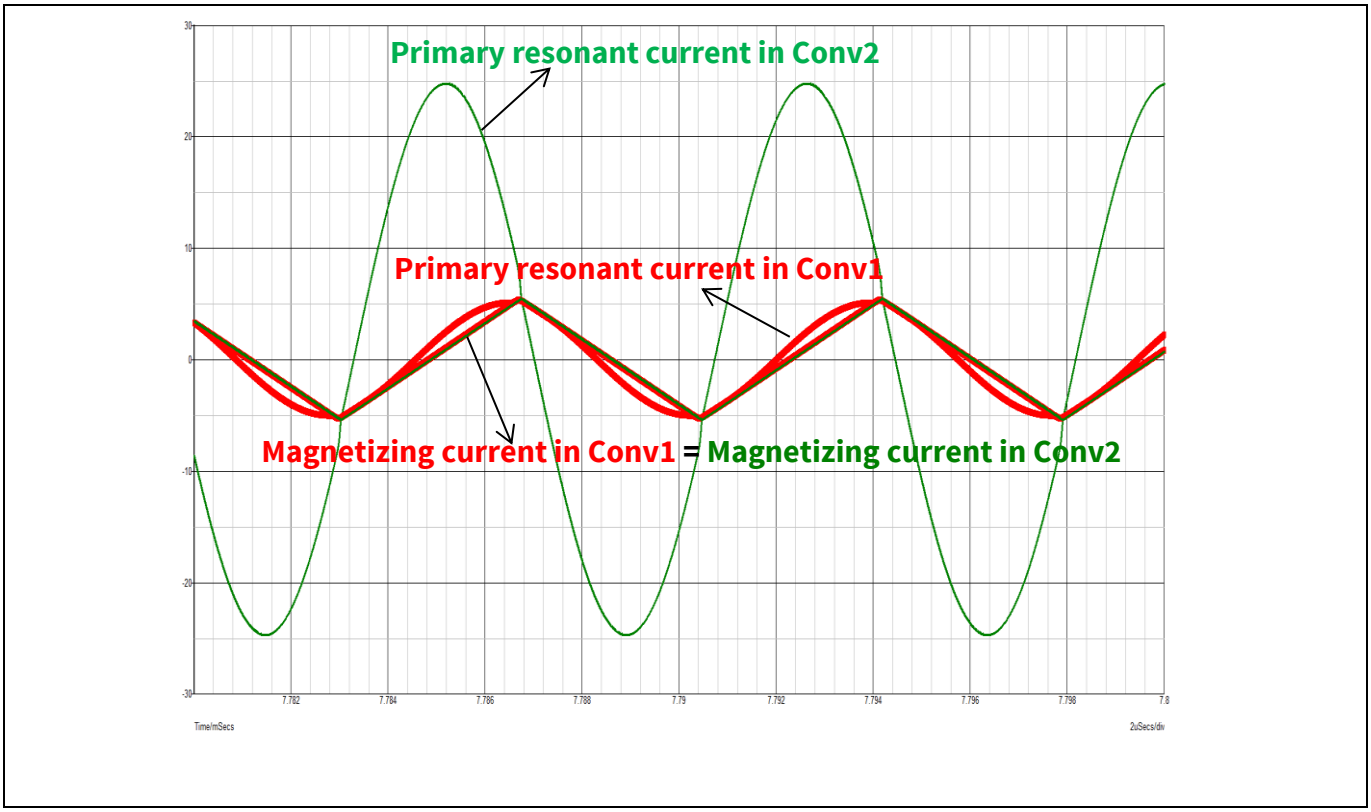



**Figure 4 Resonant and magnetizing currents in case $L_{r2}$ is 5% smaller than $L_{r1}$**

This small difference already generates a pretty high imbalance in the primary $I_{res}$ of the two phases, as shown in Figure 4, while of course the two magnetizing currents are still perfectly coincident, since there is no change in the main transformers.

Basically, the reduction of $L_{r2}$ generates a reduction in the equivalent impedance of the Conv2 resonant tank. Since the $F_{sw}$ has been kept the same as in the balanced case, Conv2 shows a larger gain than Conv1 at this $F_{sw}$.

Figure 5 explains the reason for the Conv1 secondary rectified current shape in the case of $L_r$ imbalance: the current is almost totally diverted into the Conv2 resonant tank, so the $I_{res}$ in Conv1 becomes very low, almost overlapping the magnetizing current. In particular, during the time intervals when they are equal (e.g. starting from points 1 and 2 in Figure 5), the secondary rectified current becomes zero. This operation resembles the no-load operating condition and generates a secondary current in Conv1 similar to what it is expected in Discontinous Current Mode (DCM) operation, typically seen when the LLC converters operate below resonance. Actually, the Conv1 still operates at the resonant frequency, since $L_{r1}$ and $C_{r1}$ haven't been changed, but almost at no load, which is the reason why the secondary rectified current shows a discontinous behavior.

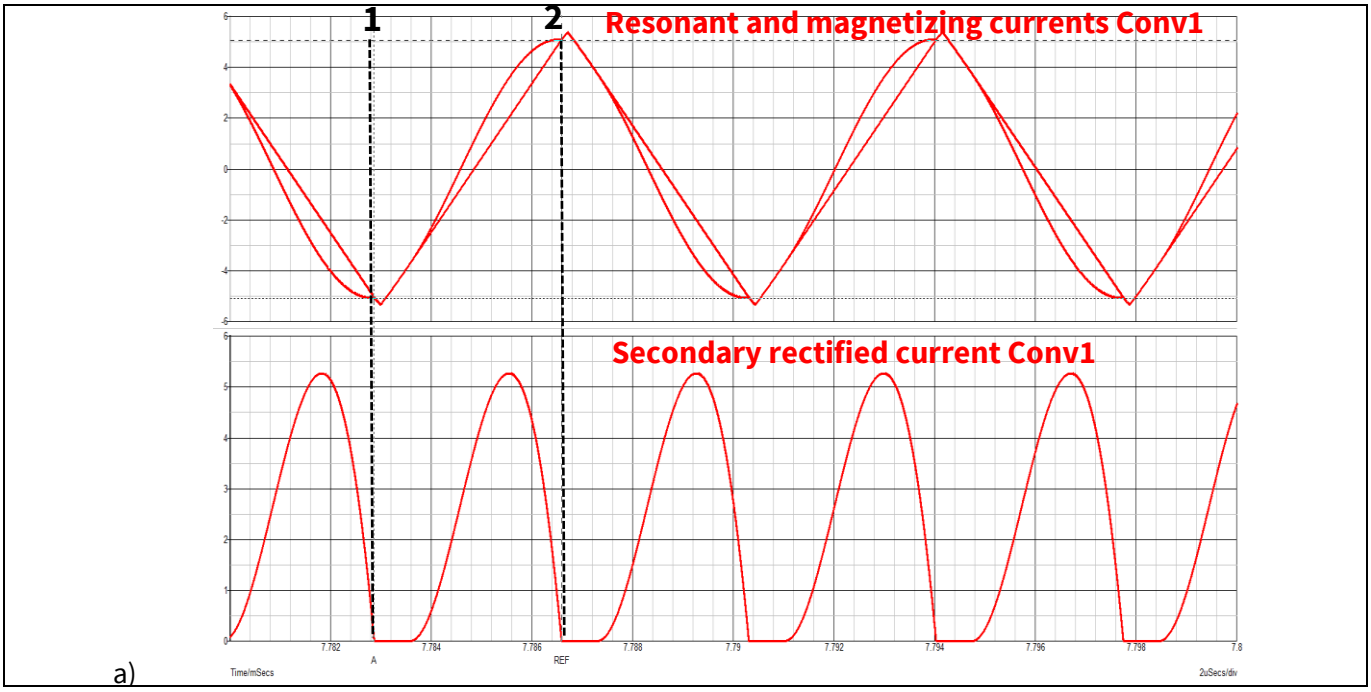



**Figure 5 Resonant, magnetizing and secondary rectified currents in case $L_{r2}$ is 5% smaller than $L_{r1}$**

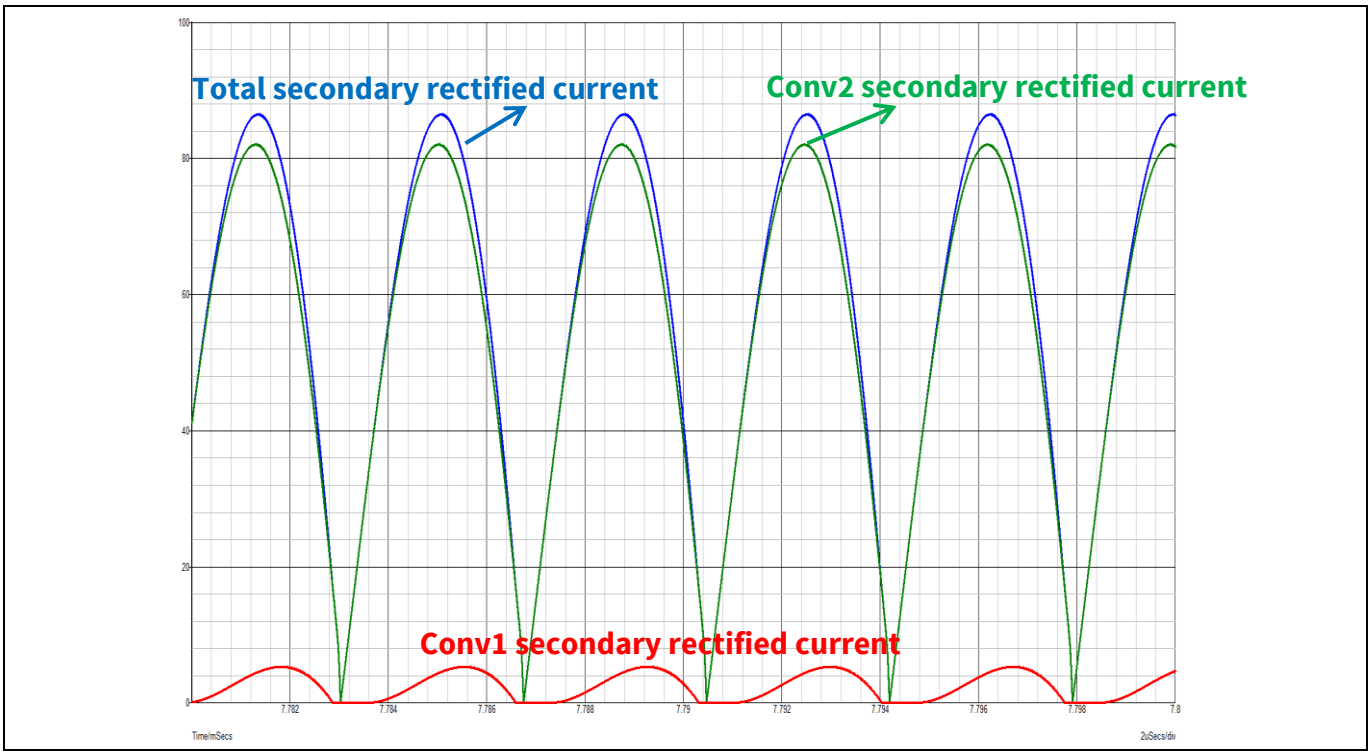



**Figure 6 Secondary rectified currents in case $L_{r2}$ is 5% smaller than $L_{r1}$**

Looking at Figure 6, you can easily understand what happens in practice. The total secondary rectified current almost corresponds to the one in Conv2, which, in other words, will get almost the entire load current. Of course, the Conv2 is typically not designed to sustain the full load of the whole dual-phase converter, since it is supposed to work only up to half-load. Therefore, it will go immediately into output over-current/over-power, thus generating the shut-down of the complete converter.

Further simulations show that a similar behavior can be observed in case of a mis-match of only 5% in the values of the resonant capacitors in the two HB LLCs.

These simple examples clearly demonstrate that the current sharing of two paralleled resonant converters is not a trivial topic and represents a real design challenge.

The technical literature suggests several techniques to avoid this issue.

The simplest is to perform a pre-selection of the resonant tank components (inductor and capacitor) in order to use identical values in the two phases. But this selection normally results in expensive and time-consuming SMPS mass production, especially for high volumes, so this solution is typically not chosen by big SMPS manufacturers.

A possible alternative solution is proposed in [2], where an additional intermediate conversion stage is added to regulate the LLC converter input voltage ($V_{in}$) in order to allow each of the two converters to always operate at the optimal frequency for current balancing. The key to this technique is to get the output regulated through the variation of the $V_{in}$ rather than the resonant stage gain. This solution avoids current imbalance, but, on the other hand, will unavoidably impact the overall converter efficiency, due to the introduction of an additional conversion stage.

Another useful solution is proposed in [3] and [4]: it consists of compensating the resonant component mis-match by means of an additional inductor with adjustable inductance value. In that approach the use of a magnetic core with saturation windings can provide an effective way of varying the value of the inductor wound on the same core. In order to be really effective, this technique requires a very precise output current measurement combined with a very accurate control of the resonant inductor value as a function of the current imbalance in two or more converter phases.

### 2.1.2 Proposed implementation

Each of the methods described above has pros and cons.

In our 3 kW dual-phase design we opted for a more traditional direct control of the converter's $F_{sw}$ as a function of the current in each of the two phases.

This technique has also several different implementations and, of course, several tricky aspects.

One of them is faced when trying to keep the two switching frequencies as close as possible. If they are very close but not exactly the same, this can result in beat frequency effects that can be critical for EMI and acoustic noise, as well as severely affecting the output ripple and thus requiring filtering. Some other techniques have the disadvantage of reducing the reliability and reproducibility of the resulting LLC converter arrangement.

In case the N-paralleled converters run at synchronized frequencies, having independent input voltages helps. However, this requires a separated PFC for each of the paralleled LLCs, which can increase the complexity of the PFC control. This solution does not give effective ratio efficiency vs cost and power density. Cost and power density are important considerations in modern high-power SMPS design.

In some cases, one converter is voltage controlled and the other (N-1) is current controlled, where the value used by the current controller is the output current of the voltage-controlled converter: a main drawback is that this can make the N LLC loops unstable.

Our 3 kW dual-phase LLC design concept is able to overcome load imbalance between the two HB LLC converters while maintaining good reliability, reproducibility and efficiency.

The converter consists of two HB LLCs, each with its transformer, resonant choke and SR stage. A microcontroller located in the secondary side takes care of the control of both converters.

## Dual-phase HB LLC design concept

Figure 7 shows the general operational principle of the current sharing, by acting on the $F_{sw}$ of one of the two converters. The so-called “phase shedding” function is also included, which consists of the switching-off one of the two converters below a certain load.

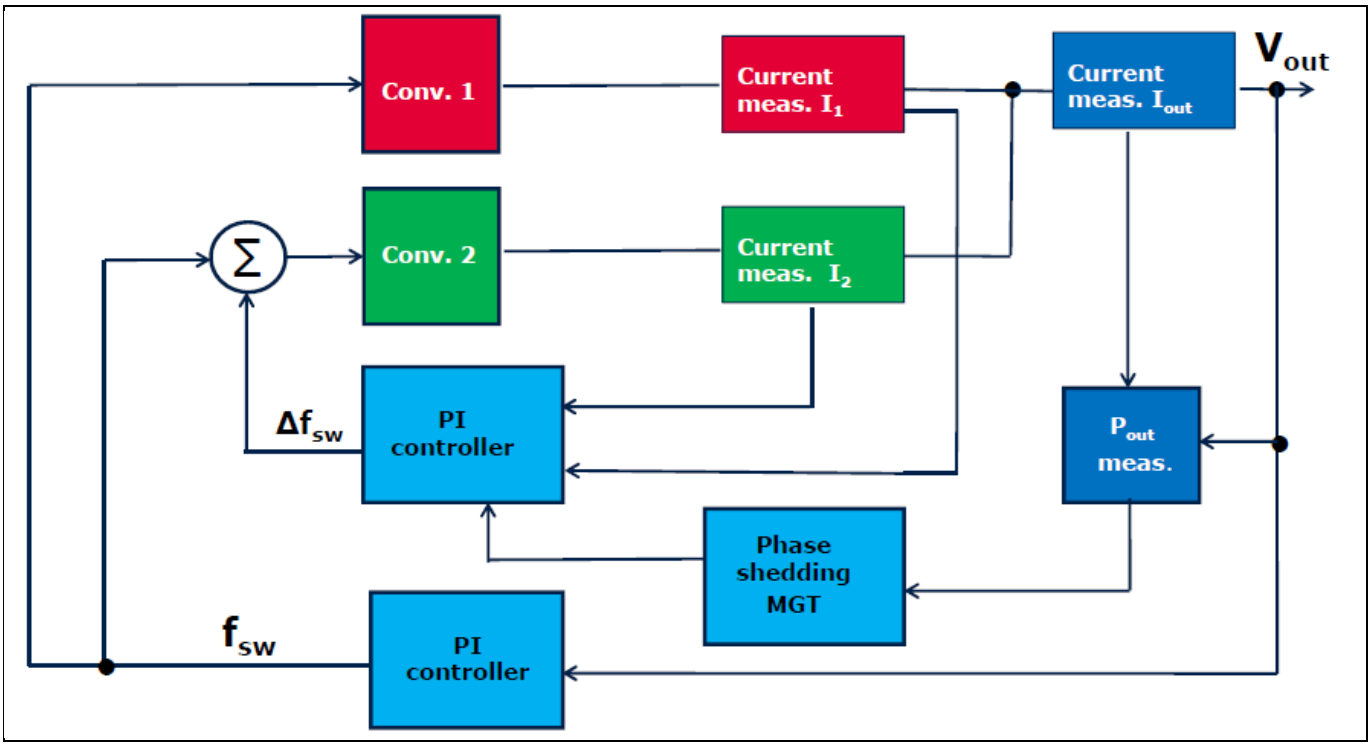



**Figure 7 General current-sharing principle of operation**

In our approach, the two phases are treated separately, so the controller peripherals must accommodate the two phases’ requirements in terms of PWMs and ADCs. The two converters may have parts tolerance/mis-match, resulting in different resonant frequencies; therefore, a separate PWM module is needed for each of the stages in order to modulate them separately to achieve current sharing.

The switching frequencies of the two LLCs are not the same, and the secondary current ripple cancelation is not guaranteed. The output ripple will increase until it reaches a maximum value when the two stages are in phase, then decreased until reaching a minimum value when the two stages are 90° out of phase. The ripple cancelation is in fact not in the main focus of our design, due to the relatively low output current (max. 55 A). Of course, the output current ripple reduction becomes more critical in the case of power converters with low output voltage ($V_{out}$) and high output current: in those cases the interleaving by phase-shift of the respective PWM paths is recommended.

The key concept of our control method is to split the output of the voltage controller into two or more control signals for the converters using the special balancing function. The balancing function is responsible for maintaining the highest efficiency in steady-state operation and prevents overloading of one of the two phases during quick power changes for dynamic regulation.

In Figure 8 you can find a schematic description of our implemented current-sharing method, which will be described in more detail in Section 4.

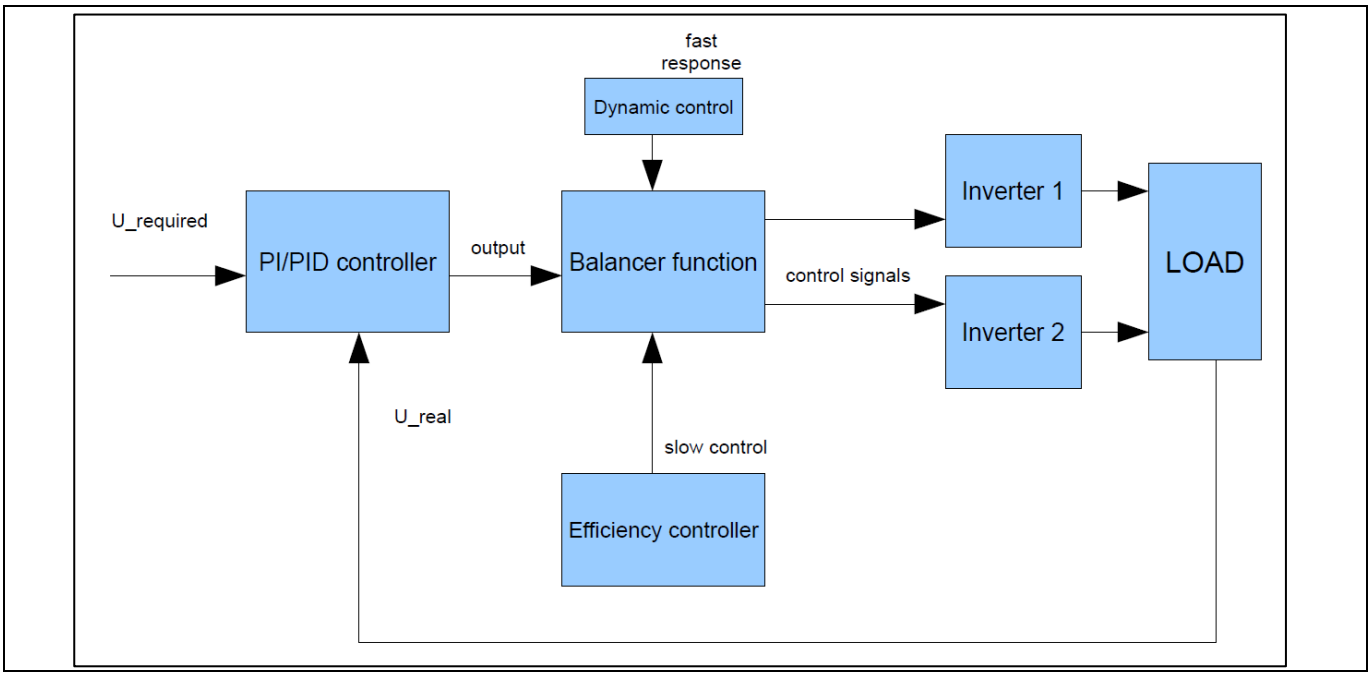



**Figure 8 Implemented current-sharing control**

The implemented algorithm is also able to switch off one of the two phases below a certain output load, to guarantee a very flat efficiency plot across the entire load range. This technique is typically combined with current sharing among two or more converters working in parallel, and is known as phase shedding.

The importance of this feature is made clear in Figure 9, which shows the typical operating time distribution of an HP SMPS used in telecom or industrial applications.

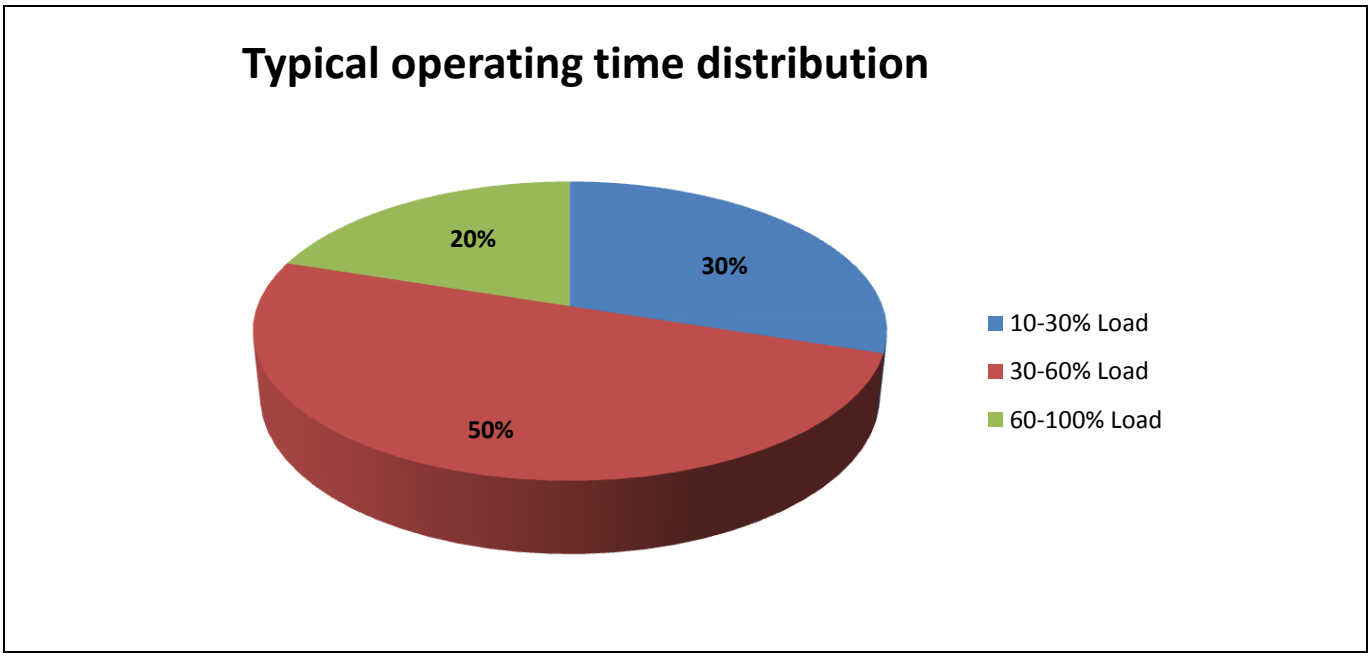



**Figure 9 Example of operating time distribution of a typical 3 kW power converter for telecom or industrial application**

You can see that on average the most significant part of the operating time is spent in the 30–60% load range. The power supply also works for a considerable time in the 10–30% range, especially in an N + 1 redundant system.

The operation close to full load accounts for a relatively small part of the time: hovewer, we know that this is the most critical part from a thermal perpective, so special care must be taken with it.

The multi-phase with phase-shedding approach addresses the requirements of high efficiency not only at mid-load (which is the “natural” behavior of a single-phase converter), but also a light and heavy load, making possible the aforementioned flatness of the efficiency plot.

The performance achieved in the present demo board is described in detail in Section 5 of this document. In that section you’ll see the crucial contribution of the power devices, especially the new 600 V CoolMOS™ CFD7 family, along with the control technique made possible by the XMC™ controller.

To complete the introduction to our concept and corroborate its effectiveness, Figure 10 shows the final efficiency plot achieved. You can see the very high peak efficiency, but also the very flat plot over the entire load range. The low driving and switching losses of the 600 V CoolMOS™ CFD7 technology are the key enablers of the very high efficiency at light load of each single HB LLC converter (or phase). The phase shedding is the other key contributor at light load. The flatness from medium to full load is the result of the excellent Figure of Merit (FOM) $R_{DS(on)}$* switching losses of CFD7.

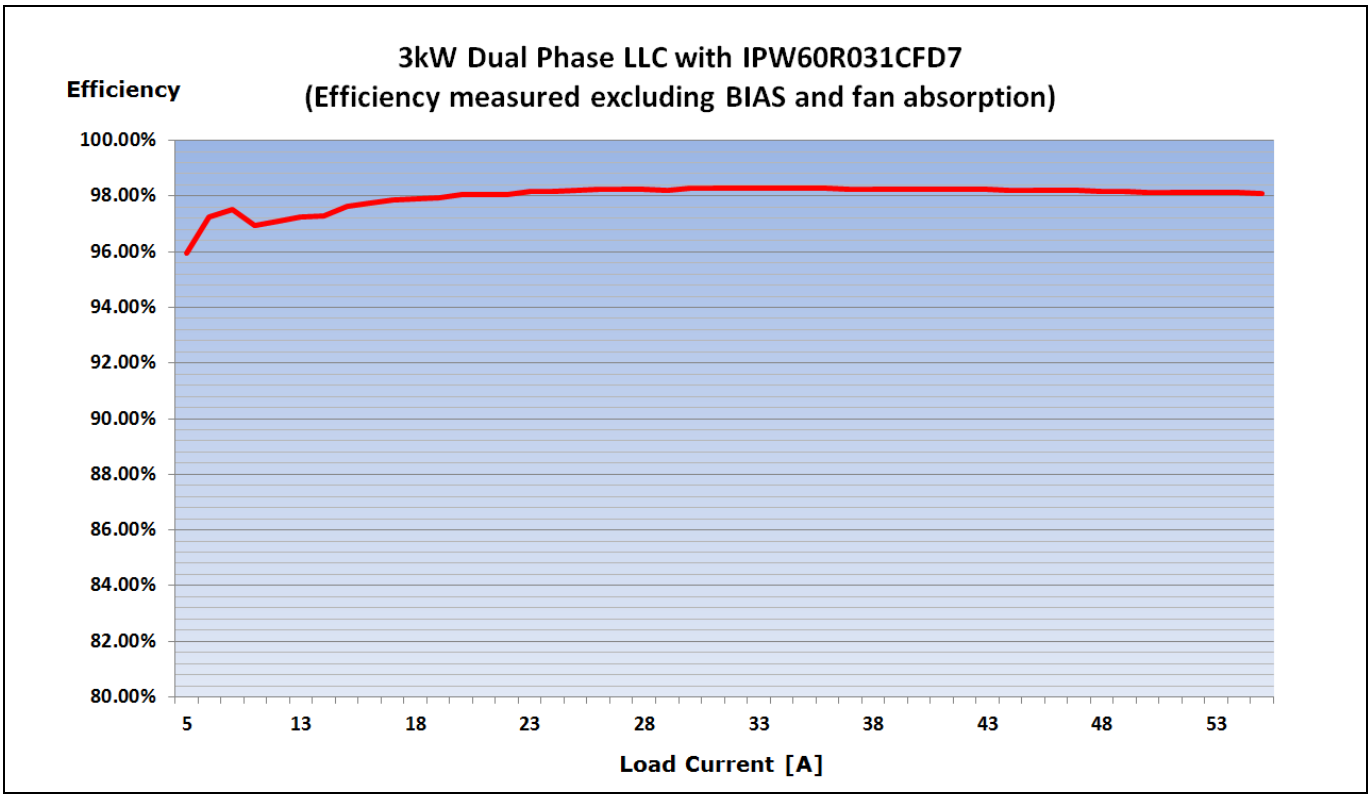



**Figure 10 600 V CFD7-based 3 kW dual-phase LLC efficiency plot**

## 2.2 Reliability features

The critical operating conditions of an HB LLC converter are well known in the SMPS designers’ community.

In fact, although knowledge of the HB LLC topology has significantly improved in the last 10 years, these critical operations often still discourage SMPS designers from using this solution for high-efficiency power converters where reliability matters. In fact, these conditions are considered particularly challenging, since they might

occur in SMPS mass production, even in the field, despite the fact that this has never been reproduced in the lab tests during the design and qualification phase. Customers perceive this as extremely risky. Moreover, there are several studies showing that there is a huge difference in the cost of fixing an SMPS problem at different stages: e.g. the cost to fix it in the field/at the final customer site is 1000 times higher than during the design phase.

These tricky operating conditions of the HB LLC converter have already been analyzed in [1].

In a dual-phase approach these problems are expected to be further amplified due to the synchronization of the two phases, which can be critical, especially during dynamic operation. So, special care must be taken with those aspects when designing LLCs in a multi-phase approach.

It is worth recapping the main problems that can occur in these critical operating conditions, before introducing the ways we avoid them in our 3 kW dual-phase LLC.

The best-known and most dangerous mechanism affecting LLC operation is the so-called hard-commutation on the conducting MOSFET BD. This typically occurs during the start-up sequence (illustrated in Figure 11), but also during burst mode or output short-circuit, and can lead to failure of the HV power devices in the primary side of the converter.

This problem occurs when one of the two MOSFETs in the HB LLC configuration (Q2 in Figure 11) is turned off while its BD is still not completely reverse-recovered. If this happens, when the other device (Q1) turns on, the MOSFET Q2 is submitted to heavy stress, since the $V_{O,PFC}$ voltage is applied between its drain and source while a huge reverse current is flowing through the BD, creating a shoot-through effect. This stress can result in Q2 device failure, and Q1 may also be damaged. A very similar mechanism can be triggered during burst mode operation. The root cause of this behavior is the initial imbalanced voltage across the resonant capacitor, which leads to flux imbalance on the primary-side transformer.

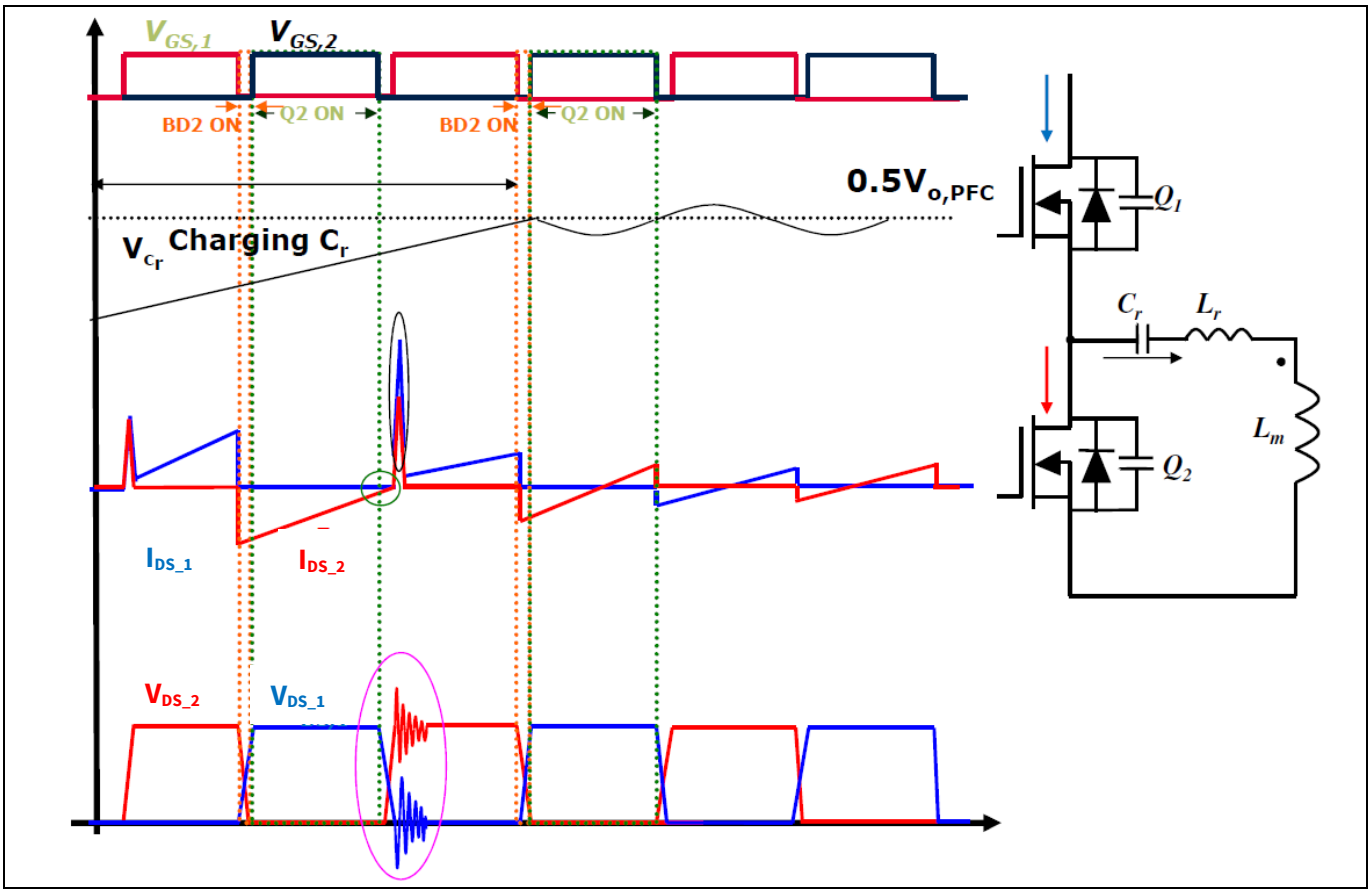



**Figure 11 Hard-commutation during HB LLC start-up sequence**

### Dual-phase HB LLC design concept

Hard-commutation may be also experienced during load dump in conjunction with secondary-side Synchronous Rectification (SR): a feedback (FB) of energy from the secondary side to the primary side may occur, which leads to reversal of tank current and thus to hard-commutation on the primary MOSFETs.

In general, hard-commutation happens everytime the $I_{res}$ “leads” the resonant voltage, so that the voltage is in the mid-point of the HB: this specific condition is well known as “capacitive load mode operation” of the LLC converter.

There are several ways to prevent hard-commutation in the HB LLC topology. Some of them are “by design” (like the use of the so-called “split capacitor technique”). Actually it is impossible to precisely predict and avoid this condition by the converter design (e.g. LLC gain curves shape), without using a dedicated control strategy.

We decided to use a dedicated control strategy to prevent hard-commutation in all the possible triggering events, not only at start-up or in the case of output over-load, but in all those conditions, unpredictable by design, where the $I_{res}$ may potentially “lead” the resonant voltage.

The proposed control is fully digital and is located on the secondary side, which has a couple of benefits in terms of transient response and output current measurement. The $I_{res}$ is guaranteed to lag behind the resonant voltage: in fact the control is placed in the secondary side, but the primary-side tank current is continuously monitored by using a current transformer to provide the necessary reinforced isolation.

The start-up and burst mode sequences are based on the Zero Crossing Detection (ZCD) of the tank current, which is implemented totally inside the microcontroller without additional external hardware components (e.g. comparators). By detecting the tank current ZC the control ensures change of polarity of the tank current and thus current reversal in the main transformer. The four steps included in the start-up sequence are explained in detail in Section 4.

The algorithm implemented also includes an additional procedure that is able to detect load dump and prevent energy flow from the secondary side to the primary side. The control measures the output current and detects a negative slope in the measured current (-di/dt), which indicates a fast decrease of load current. If a negative slope is detected, a dedicated SR control is applied.

Special care is needed in the management of the capacitive load mode condition, because this is recognized to be the most critical and often most unpredictable HV MOSFET failure mechanism in the LLC topology.

Our algorithm is able to both predict and protect against this. The control measures the phase-shift between the resonant voltage and $I_{res}$. Measurement for phase-shift can be implemented by counting the time from the MOSFET turn-off of the previous period until the tank current reverses (see Figure 12).

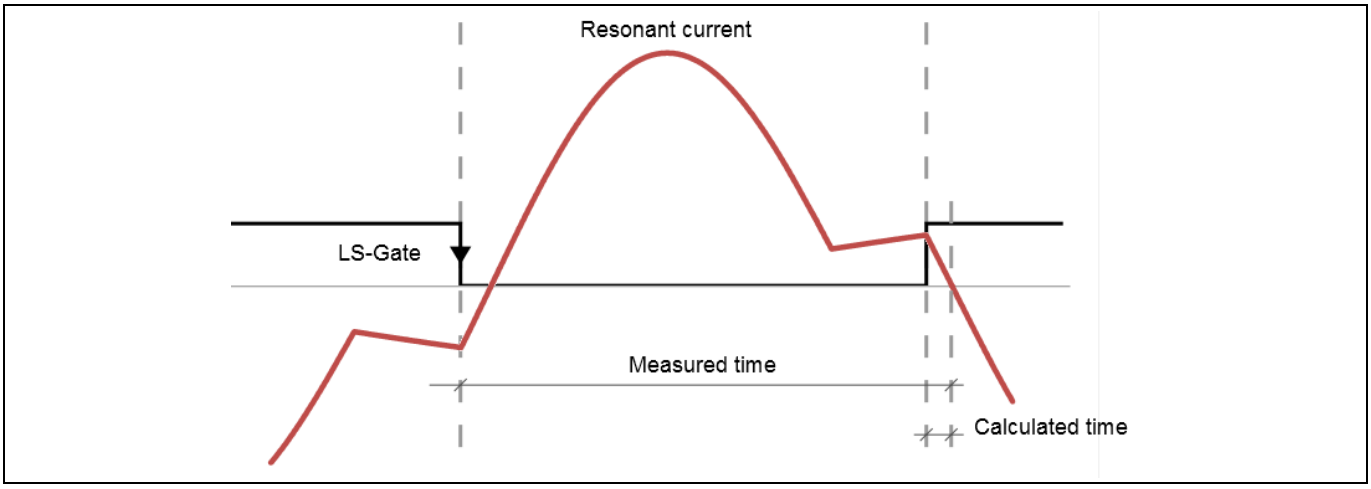



**Figure 12 Capacitive load mode prediction and protection concept**

The phase-shift is calculated from the measured time, dead time and $F_{sw}$. If the phase-shift becomes zero, the operation point is close to the capacitive mode. The control increases $F_{sw}$ to keep the operation point in the inductive region. This is the predictive or preventive feature implemented in our control. If a negative phase-shift is sensed, it means that capacitive mode has already occurred, and failure can be then prevented by simply turning off the MOSFET and not turning on the other MOSFET in the next half-cycle. The HB is also temporarily stopped as a precautionary measure to let the tank current decay to zero, and allow time for the switch node to bounce and the BD of the MOSFET to fully recover: this is the failure protection feature of our algorithm.

This paragraph has described the techniques implemented in the control of the 3 kW dual-phase LLC demo board in order to prevent/protect against hard-commutation on BDs that are not fully recovered. It has been shown [11] that this occurrence is more likely in HP converters, where MOSFETs with low $R_{DS(on)}$ are used. As a general rule, devices with $R_{DS(on)}$ less than 100 mΩ are more prone to this problem in LLC applications. In that case, an additional safety margin is provided by the use of a MOSFET with fast BDs, which physically minimizes the reverse minority current in the “shoot-through” effect described above, thus significantly reducing the risk of failure.

In conclusion, the combination of a device like the new CoolMOS™ 600 V CFD7 and the accurate control algorithms gives full confidence about the converter’s reliability, without sacrifying any performance.

## 2.3 Graphical User Interface (GUI)

A Graphical User Interface (GUI) has been designed as complementary tool for the 3 kW dual-phase LLC design, with the purpose of enabling easy and intuitive interaction with the power converter.

The GUI enables the user to set some of the converter’s electrical parameters, such as the value of the $V_{out}$, maximum output current and the related OCP threshold.

Moreover, the GUI provides continuous monitoring of the converter’s operation, including $V_{in}/V_{out}$ and current or temperature on the transformer of both phases. Several status and fault registers are visible, allowing for an immediate understanding of the reason for a fault condition.

The user may need to customize the operation of the board to their specific needs. For this reason the GUI makes it possible to re-configure the topology, e.g. by completely switching off one of the two phases, then limiting the maximum power to 1.5 kW. It is also possible to disable the SR stage, in case fine-tuning is required using only MOSFET BD rectification.

The GUI is able to automatically calculate the dead times as a function of the output capacitance ($C_{OSS}$) of the different MOSFETs used in the HB LLC: this enables design optimization according to the different MOSFETs used in the primary side, with the goal of guaranteeing ZVS behavior across the entire load range.

The user can also adjust the converter’s transfer function in order to optimize dynamic performance and loop stability.

The hidden and abstracted control concepts can be understood in a very precise and effective manner by means of a GUI. In fact, before the implementation of the control-loop design, a simulation is essential. This should prevent design problems arising during hardware implementation, when there will be limited room for maneuver. On the other hand, achieving an optimal response through simulation requires certain skills in control system theory; the precise positioning of poles and zeros in the compensator is not easy for less-experienced designers. Moreover, the loop compensation is also heavily influenced by the total amount of $C_{OSS}$, including that applied outside the PSU. This additional capacitance often changes from case to case, even for the same PSU.

### Dual-phase HB LLC design concept

To help designers with this tedious part of their job, the GUI provides a menu where the total amount of additional external $C_{oss}$ can be set, and then the algorithm will automatically re-calculate the poles and zeros of the transfer function for loop stability, by fulfilling the technical specification requirements:

| | |
|---|---|
| Phase margin: | min. 45°C @ 0 bode plot gain crossover frequency |
| Gain margin: | min. 10 db @ 0 bode plot phase crossover frequency |

A more detailed description of the GUI functions is included in Section 4.8.

# 3 Board description

The following sections provide an overview of the 3 kW dual-phase demo board, with details about the technical specifications, the electrical schematics, and the main active and passive components, including Infineon power devices and ICs, and magnetic parts.

## 3.1 Main requirements in the technical specification

- $V_{in}$ range 350 $V_{DC}$ to 410 $V_{DC}$
- Nominal $V_{in}$ 380 $V_{DC}$
- $V_{out}$ 44 V to 58 V ±1%
- Nominal $V_{out}$ 54 $V_{DC}$
- Max. output current/power 55 A/3000 W
- Dual-phase approach
- Power density > 30 W/inch$^3$
- Efficiency target: 10/50/100% $P_{max}$ = 95%/98%/97.5%

## 3.2 General overview of the final design

Figure 13 shows the basic structure of the 3 kW dual-phase LLC design.

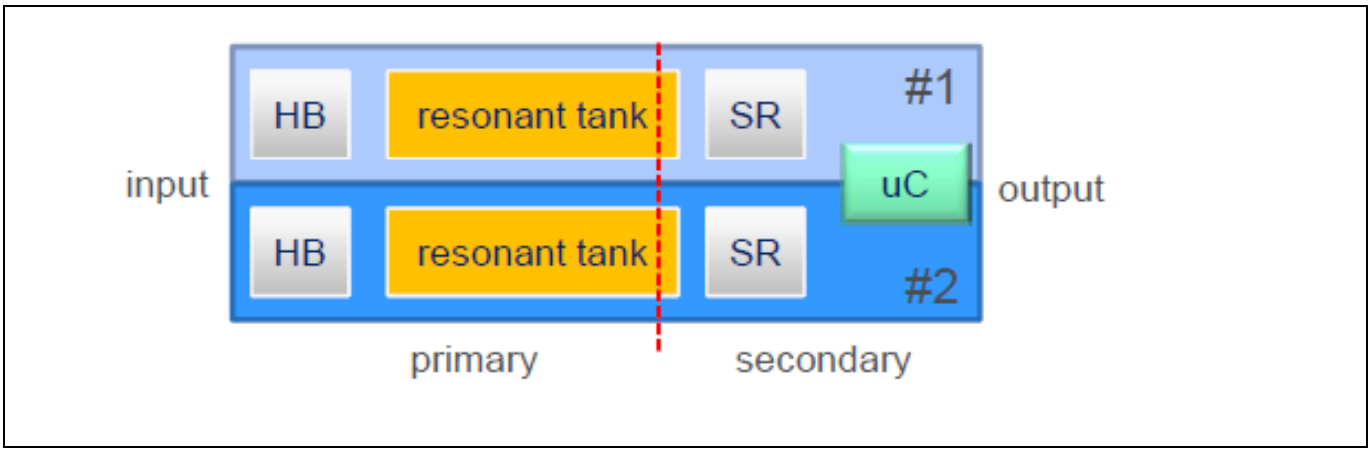



**Figure 13 3 kW dual-phase LLC: basic concept**

The board consists of two HB LLC converters working in parallel: each of them has its own resonant tank and SR stage. For the sake of simplicity, we'll call these converters Conv1 and Conv2, as in the simulation described in the previous section. A single microcontroller located in the secondary side controls both converters. It generates the PWM signals for both primary and secondary MOSFETs and manages the current sharing and all the advanced fetaures, which will be analyzed in depth in the Section 4.

Figure 13 shows a real picture of the 3 kW dual-phase LLC demo board and highlights the position of the most significant components, including of course the Infineon products used.

A main power board and two daughter cards are visible in Figure 14. In the main board all the power components are assembled, including MOSFETs and magnetic parts. The first daughter card hosts the microcontroller and the related logic circuitry, so this is identified as the control card. The second daughter board (bias card) hosts the auxiliary converter, which is done with a QR Flyback converter: as is typical in HP SMPS, this small converter provides the voltages needed to supply the logic circuitry and the two ventilators, also visible in Figure 14.

Section 3.3 gives an overview of the Infineon components that have been used in the present design, highlighting their main feautures. Section 3.4 will go into the details of the electrical schematics and the magnetic component specifications.

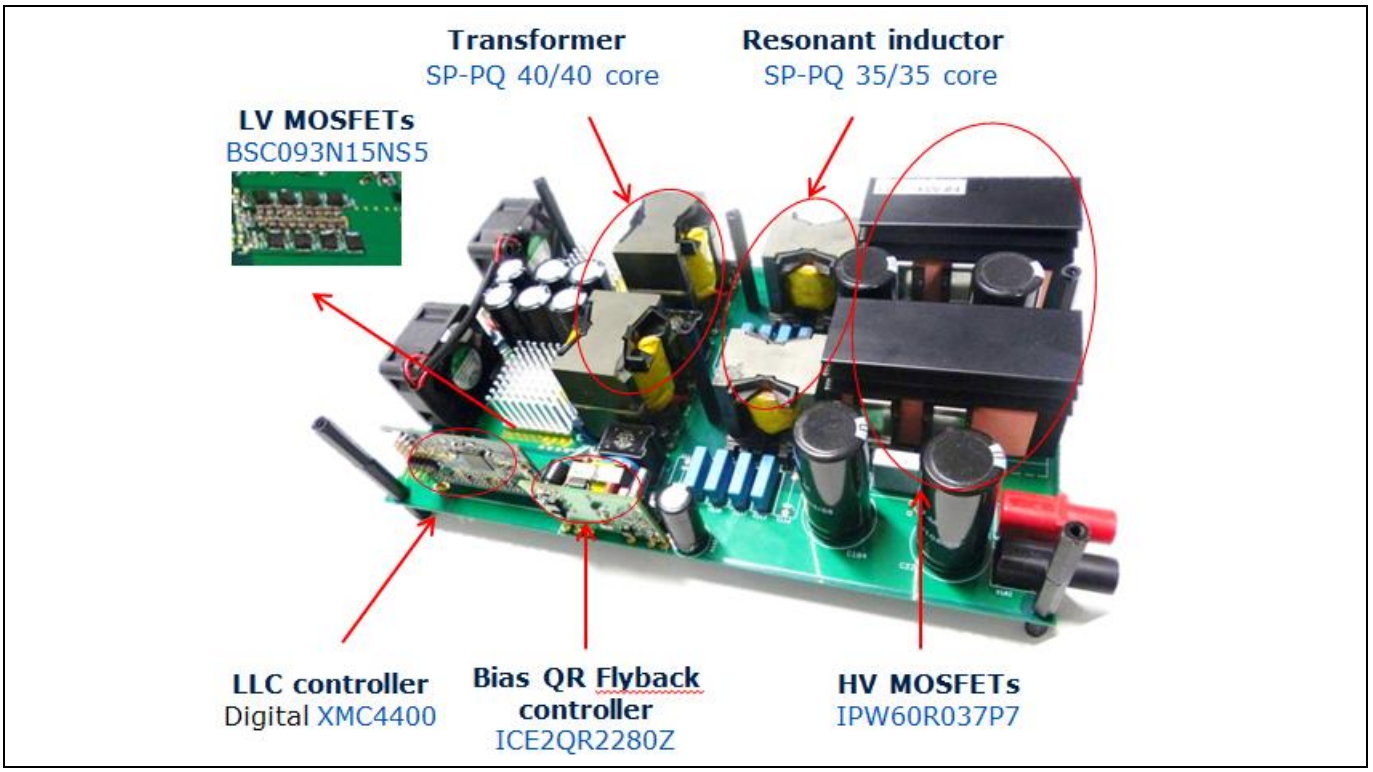



**Figure 14 The 3 kW dual-phase LLC demo board**

## 3.3 Infineon components

### 3.3.1 Primary HV MOSFETs CoolMOS™ CFD7 600 V

CoolMOS™ is a revolutionary technology for HV power MOSFETs, designed according to the SJ principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series, and is an optimized platform tailored to target soft-switching applications such as phase-shift full-bridge (FB) ZVS and LLC. Resulting from reduced gate charge ($Q_g$), best-in-class reverse recovery charge ($Q_{rr}$) and improved turn-off behavior, CoolMOS™ CFD7 offers the highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast-switching technology together with superior hard-commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets the highest efficiency and reliability standards and also supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.

Features:

- Ultra-fast BD
- Low gate charge
- Best-in-class reverse recovery charge ($Q_{rr}$ )
- Improved MOSFET reverse diode dv/dt and di/dt ruggedness
- Lowest FOM $R_{DS(on)}$*$Q_g$ and $R_{DS(on)}$*$E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

- Qualified for industrial-grade applications according to JEDEC (J-STD20 and JESD22)

Benefits:

- Excellent hard-commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use/performance trade-off
- Enabling increased power density solutions

Applications:

- Suitable for soft-switching topologies
- Optimized for phase-shift FB (ZVS), and LLC stages in server, telecom and EV charging applications

### 3.3.2 Isolated gate drive 1EDI60N12AF

The Infineon EiceDRIVER™ 1EDI Compact family consists of a single-channel HV gate driver IC with integrated Coreless Transformer (CLT) technology and a maximum offset voltage of 1200 V. The 1EDI Compact driver ICs are available in a compact PG-DSO-8 (150 mil) package and provide either separated source/sink outputs or a single output with an additional clamping function.

Summary of the 1EDI60N12AF features:

- Separate source/sink output
- $I_{out}$: 6 A @ 15 V
- 1200V Coreless Transformer IC with galvanic isolation
- Prop. delay < 105 ns with 40 ns input filter time
- High CMTI robustness > 100 V/ns

Benefits:

- Tailored to all 600 V CoolMOS™ CFD7 and P6 families, and in general for SJ MOS transistors
- High $F_{sw}$ applications as SMPS, up to 4 MHz
- Turn-off vs turn-on fine-tuning
- High reliability at small footprint

In the present demo board, the 1EDI60N12AF is used to drive the High-Side (HS) and Low-Side (LS) MOSFETs of each of the two HB LLCs. Its reduced propagation delay is an important feature in our application due to the microcontroller position on the secondary side; moreover the high CMTI and the possibility of split-source and sink outputs help to get the full benefit out of the 600 V CoolMOS™ CFD7 switching behavior.

### 3.3.3 SR MOSFETs OptiMOS™ BSC093N15NS5

The OptiMOS™ 5 150 V dramatically improved the $R_{DS(on)}$ per package for this voltage range: 9.3 mΩ is available even in the compact Super SO8 package, which has been used in the present demo board. This enables the customer to switch from the FB SR topology on the secondary side to the center-tap transformer approach, yielding simplicity in the design and cost reduction (only simple LS drivers needed instead of two HB drivers).

This is in fact the main reason why we opted for a center-tapped transformer in the present 3 kW LLC design despite the relatively high $V_{out}$.

The OptiMOS™ 5 150 V has a more linear $C_{OSS}$, and yet there is a reduced total output charge in comparison with the previous generation: this contributes to reducing any voltage overshoot.

The BD has increased ruggedness due to the reduced $Q_{rr}$ offered by the new technology: these results in reduced overshoot when the converter operates above resonance and during abnormal conditions.

Finally, the typical OptiMOS™ 5 technology very tightly matches some key parameters, like $V_{GS,th}$, which is a fundamental feature in order to guarantee a reliable SR operation, especially in a dual-phase design, where each of the phases also uses several paralleled devices in each branch.

### 3.3.4 Advanced dual-channel gate drive 2EDN7524

The fast dual-channel 5 A non-isolated gate driver is an advanced dual-channel driver optimized for both standard and SJ MOSFETs, as well as GaN power devices, in all applications in which they are commonly used. The input signals are TTL compatible with an HV capability up to 20 V and down to -5 V. The unique ability to handle -5 $V_{DC}$ at the input pins protects the IC inputs against GND-bounce transients.

Each of the two outputs is able to sink and source current up to 5 A, utilizing a true rail-to-rail stage that ensures very low impedances of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail. Very low channel-to-channel delay matching (typically 1 nS) is implemented, which enables the double source-and-sink capability of 10 A by paralleling both channels.

Different logic input/output configurations guarantee high flexibility for all applications; e.g. with two paralleled switches in a boost configuration. The gate driver is available in three package options: PG-DSO-8, PG-VDSON-8 and PG-TSDSO-8-X (size minimized DSO-8).

In the present demo board, the 2EDN7524 is used to drive the SR MOSFETs. In this application the 5 A peak current capability and the very precise channel-to-channel delay matching, along with the high reverse current capability and negative input capability, are beneficial features in order to guarantee an SR-efficient but also reliable operation. In fact the reliability and perfect delay time matching aspects are very important in the complex SR management inside a dual-phase LLC design.

### 3.3.5 XMC4400 microcontroller

The XMC4400 combines Infineon's leading-edge peripheral set with an industry-standard ARM® Cortex®-M4F core.

The control of SMPS is a strong focus for XMC™ microcontrollers, where users can benefit from features such as smart analog comparators, High Resolution (HR) PWM timers and the ARM® Cortex®-M4F DSP instruction set, including floating-point or high-precision ADCs.

As a key feature it offers an HRPWM unit with a resolution of 150 pS. This unique peripheral makes it especially suitable for digital power conversion in applications such as solar inverters as well as SMPS and Uninterruptible Power Supplies (UPS). The XMC4400 is supported by Infineon's integrated development platform DAVE™, which includes an IDE, debugger and other tools to enable a fast, free-of-charge and application-orientated software (SW) development.

Summary of XMC4400 features:

- ARM® Cortex®-M4F, 120 MHz, incl. single-cycle DSP MAC and Floating Point Unit (FPU)
- 8-channel DMA + dedicated DMA for USB
- CPU frequency: 120 MHz
- High ambient temperature range: -40°C to 125°C
- Wide memory size options: up to 512 kB of Flash and 80 kB of RAM
- HRPWM, allowing PWM adjustment in steps of 150 ps
- 12-bit ADC, 2 MSample/sec. flexible sequencing of conversions including synchronous conversion of different channels

- Fast and smart analog comparators offer protections such as overcurrent protection, including filtering, blanking and clamping of the comparator output. A 10-bit DAC with a conversion rate of 30 MSamples/sec provides an internal reference for the comparators that can be configured to be a negative ramp for slope compensation purposes
- A flexible timing scheme due to CCU timers and HRPWM (High Resolution PWM). . These timers allow the creation of almost any PWM pattern and synchronize PWM signals with ADC measurements accurately
- Interconnection matrix to route different internal signals from one peripheral to another. For example, the comparator output can connect to a PWM timer to indicate an OCP event and immediately switch off the PWM output
- Communication protocols supported include USB, UART, $I^2C$, SPI
- USB 2.0 full-speed device
- Package: PG-LQFP-64

### 3.3.6 Bias QR Flyback controller ICE2QR2280Z

ICE2QRxxxx is the second-generation quasi-resonant PWM CoolSET™ with power MOSFET and start-up cell included in a single-package optimized for off-line power supply applications such as LCD TVs, notebook adapters and auxiliary/housekeeping converters in SMPS. The digital frequency reduction with decreasing load enables a quasi-resonant operation down to a very low load. As a result, the average system efficiency is significantly improved compared to conventional solutions. The active burst mode operation enables ultra-low power consumption during standby mode operation, and low $V_{out}$ ripple. The numerous protection functions give full protection of the power-supply system in potential failure situations.

In the 3 kW demo board the ICE2QR2280Z is used in the auxiliary converter, which has the task of generating all the voltages supplying logic circuitry and ventilators.

The key features of the ICE2QR2280Z for use as an auxiliary converter of this LLC evaluation board are:

- HV (800 V) avalanche rugged CoolMOS™ with start-up cell
- Quasi-resonant operation
- Load-dependent digital frequency reduction
- Active burst mode for light load operation
- Built-in HV start-up cell
- Built-in digital soft-start
- Cycle-by-cycle Peak Current Limitation (PCL) with built-in Leading Edge Blanking (LEB) time
- Foldback point correction with digital sensing and control circuits
- $V_{CC}$ Under Voltage (UV) and Over Voltage (OV) protection, with auto-restart mode
- Over-load/open-loop protection with auto-restart mode
- Built-in over-temperature protection with auto-restart mode
- Adjustable output overvoltage protection with latch mode
- Short-winding protection with latch mode
- Maximum on-time limitation
- Maximum switching-period limitation

## 3.4 Board schematics

### 3.4.1 LLC switching power stage

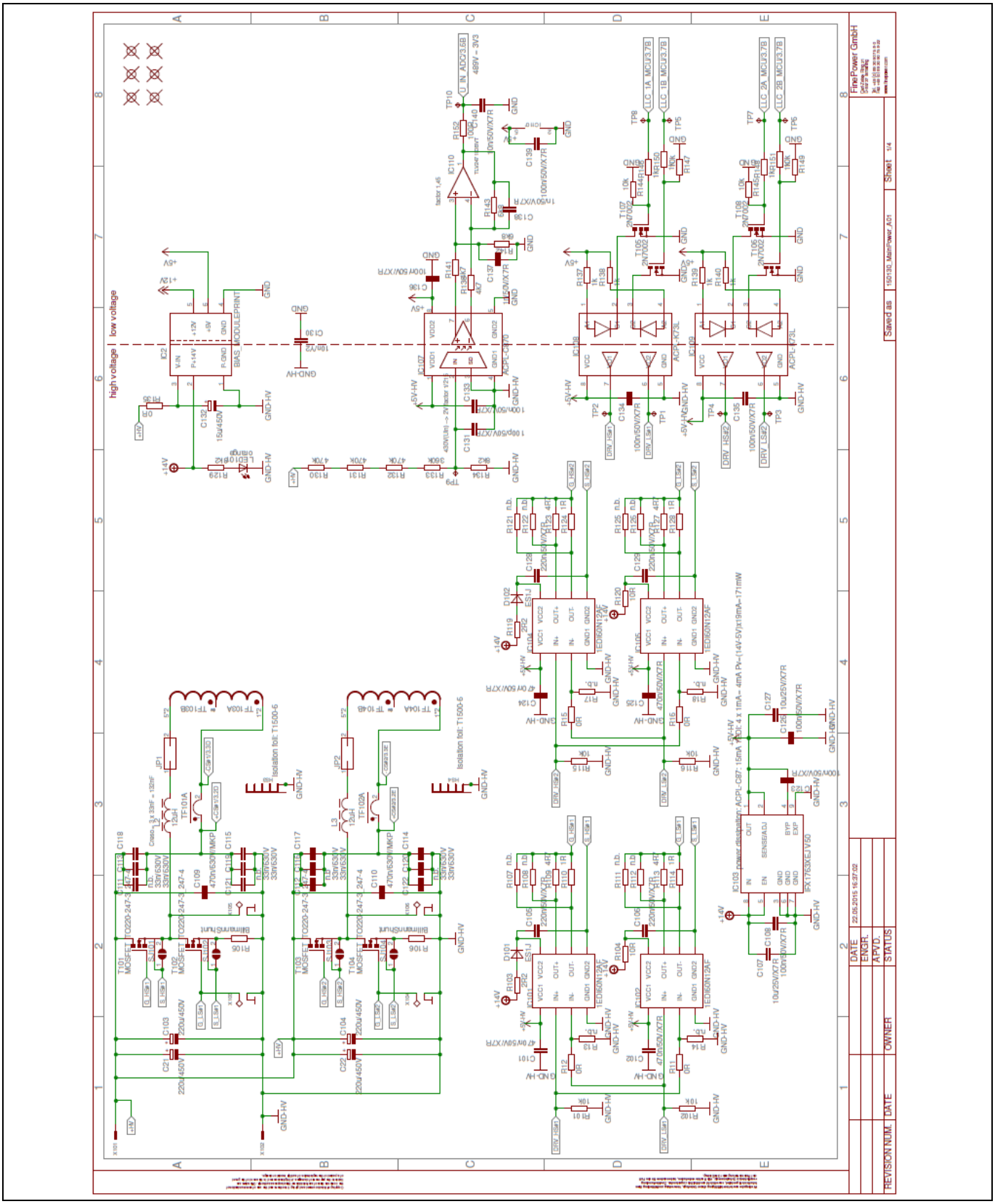



**Figure 15 Primary HV power stage**

## 3.4.2 Synchronous rectification and secondary stage

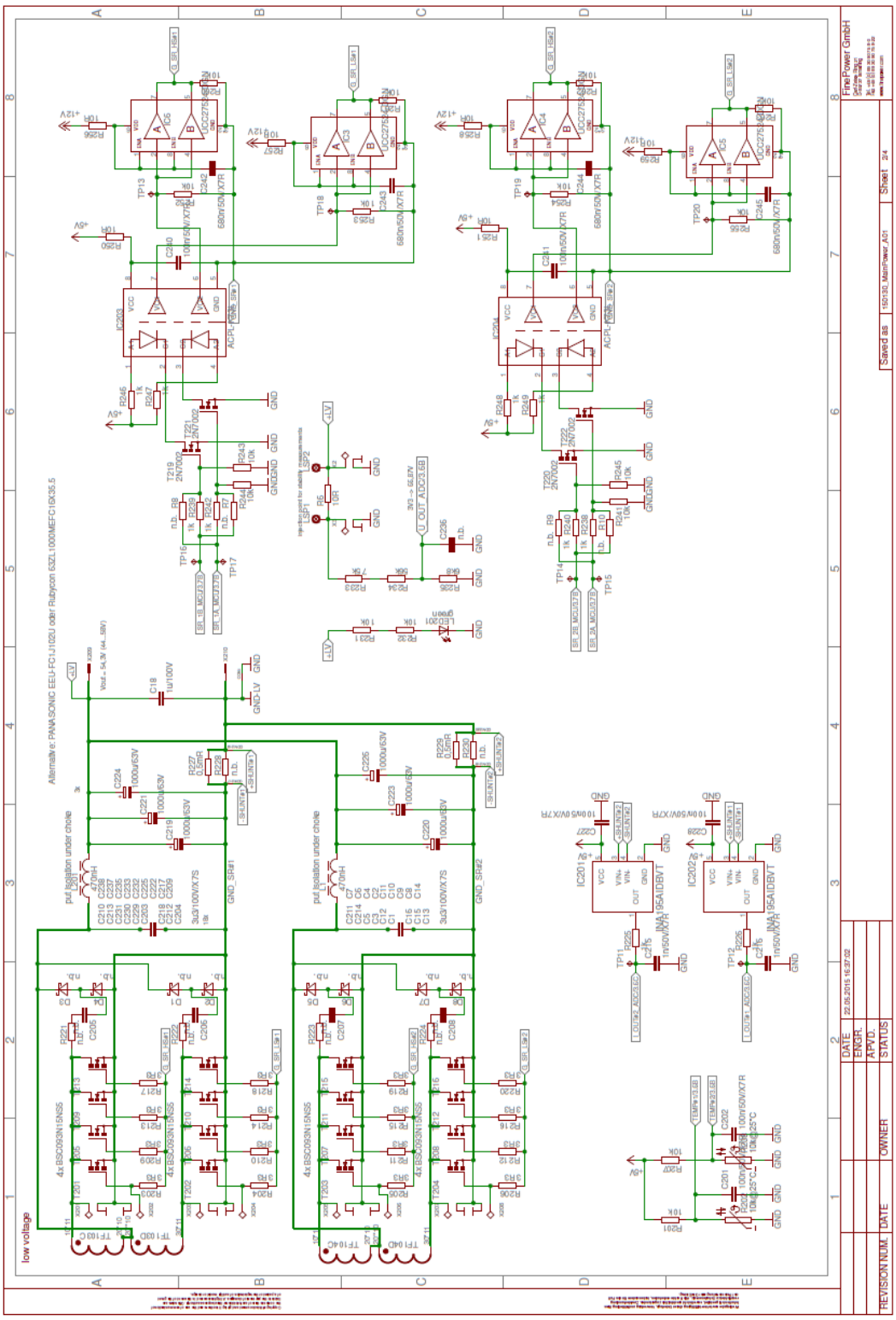


**Figure 16 Secondary-side power stage**

## 3.4.3 Control board

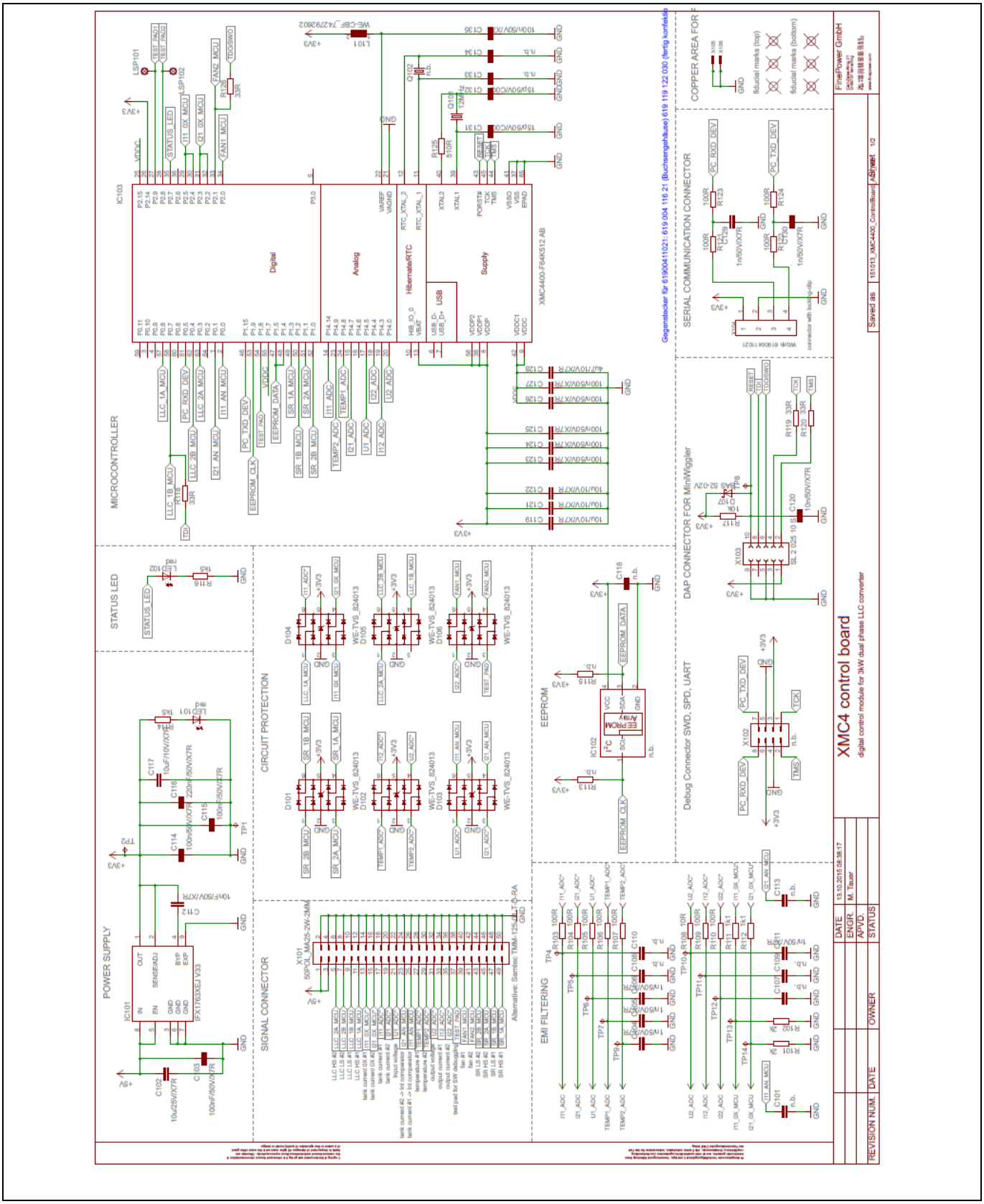



**Figure 17 Control board schematics**

### 3.4.4 Bias board (auxiliary converter)

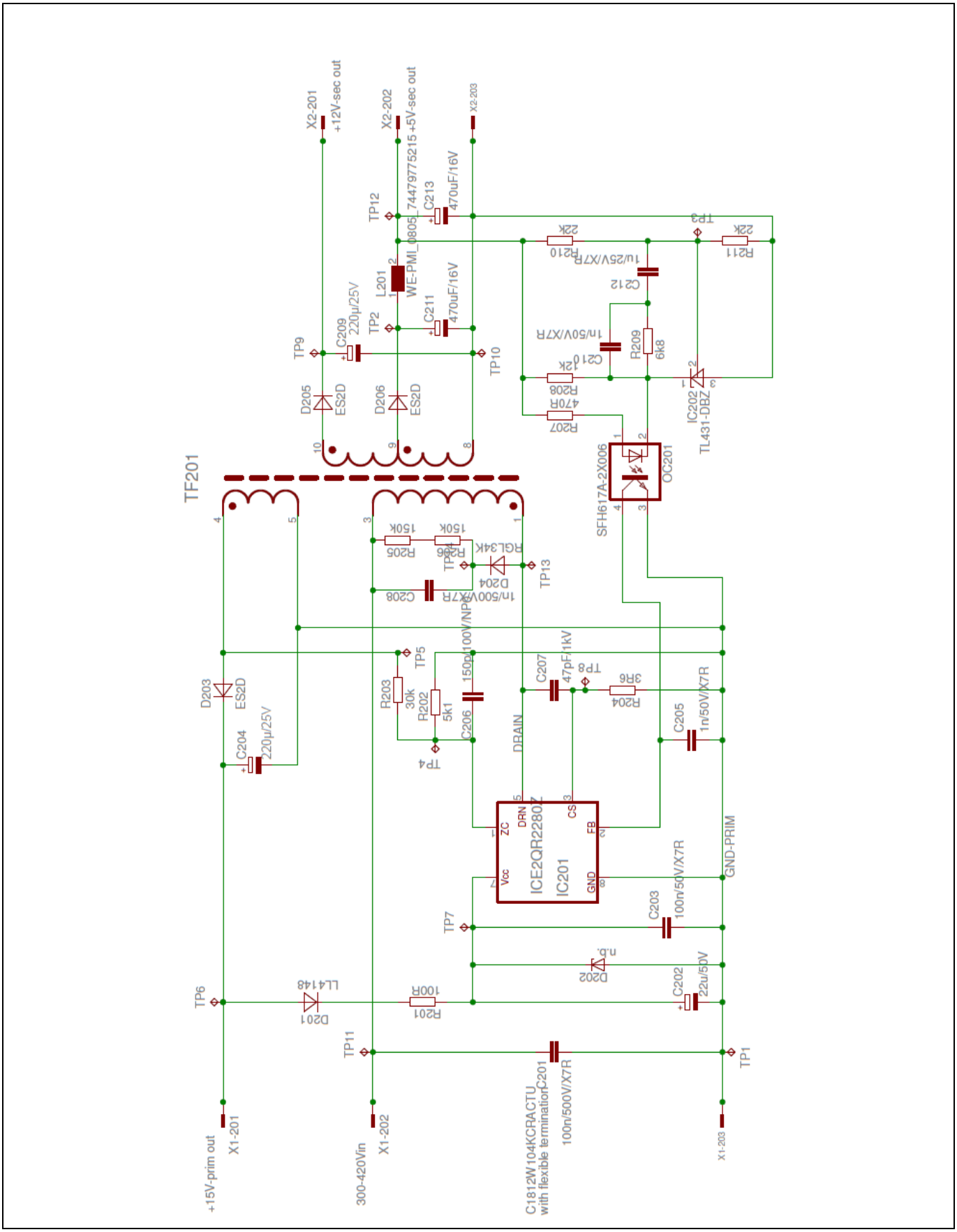
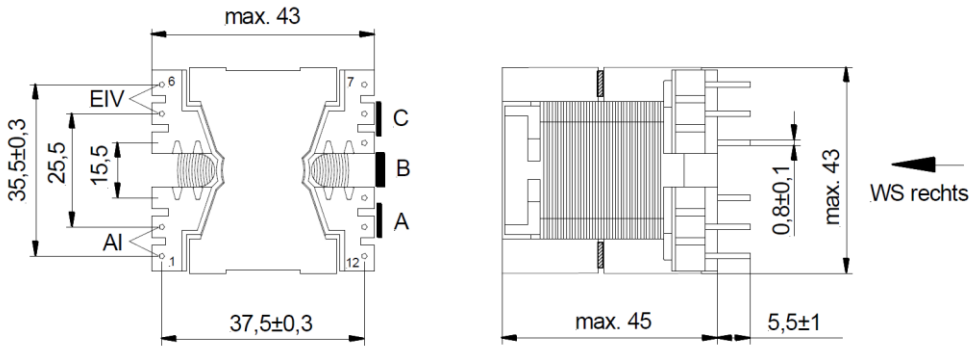


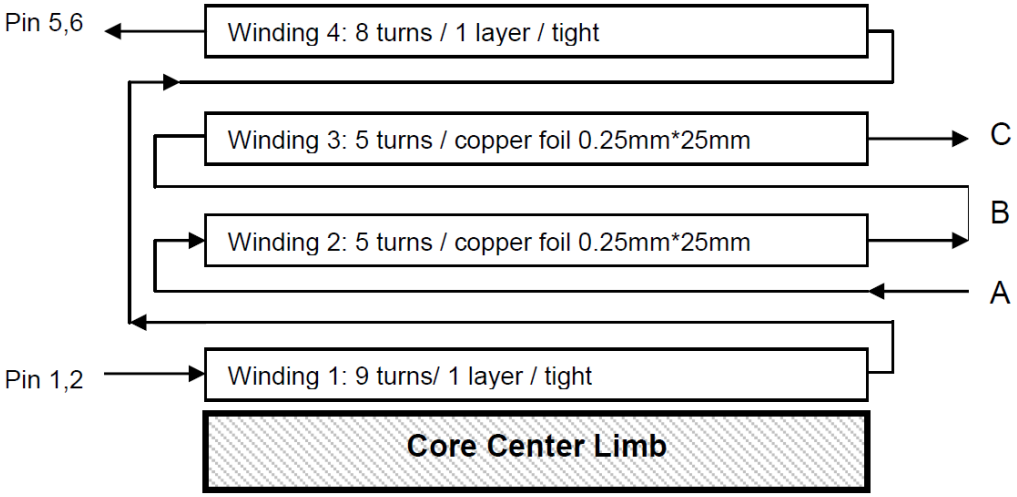

**Figure 18 QR Flyback auxiliary converter**

## 3.5 Magnetic components

### 3.5.1 HB LLC main transformer




| | |
|---|---|
| Core form and material | PQ40/40, N95 |
| Bobbin | Epcos, B65884E0012D001 |
| Primary inductance $L_p$ | 78uH, measured between 1,2 and 5,6, other pins open |
| Airgap | Distributed air gap on all three limbs |
| Leakage inductance $L_{lk}$ | 0.5uH, measured between 1,2 and 5,6, other pins shorted |
| Isolation voltage $V_{iso}$ | 2500$V_{rms}$ / 50Hz, 1min (between 1,2,3,4,5,6 and A,B,C) |

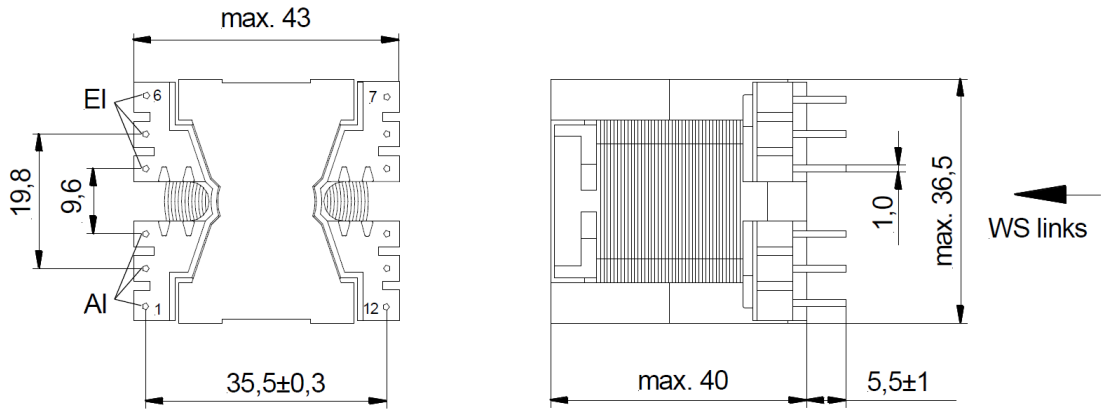



| Windings | Start | End | Wire | Turns | Layers | Method |
|---|---|---|---|---|---|---|
| 1 | 1,2 | 3 **or** float | 60x0.2mm Litz **or** 2 times 30x0.2mm Litz | 9 | 1 | Tight |
| 2 | A | B | 0.25mm*24mm copper foil | 5 | 1 | Tight |
| 3 | B | C | 0.25mm*24mm copper foil | 5 | 1 | Tight |
| 4 | 4 **or** float | 4,5,6 | 60x0.2mm Litz **or** 2 times 30x0.2mm Litz | 8 | 1 | Tight |

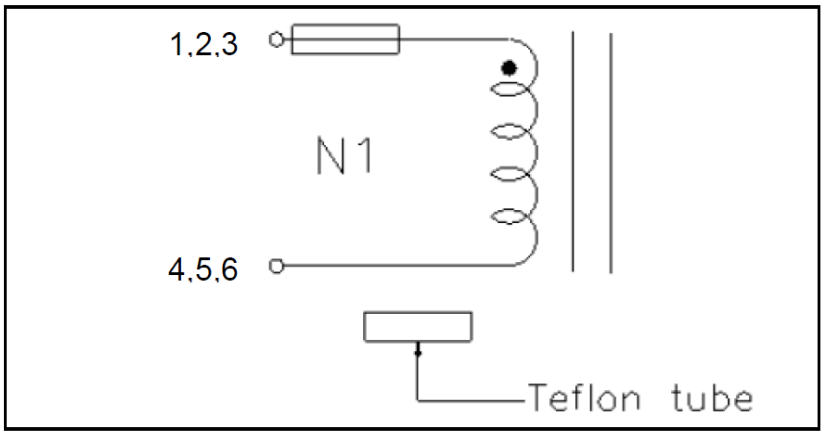
The transformer is produced by Infineon's trusted partners in the development and manufacturing of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY – http://www.kaschke.de/en/home/
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY – http://www.icetransformers.com/en/

### 3.5.2 LLC resonant choke




| | |
|---|---|
| Core form and material | PQ35/35, N95 (Epcos) |
| Bobbin | 12Pin-Standard-Bobbin<br>e.g. NORWE 90369-087 (PQ 35-35/1k/-8/mo/rtg) |
| Inductance L | 6.5 uH |

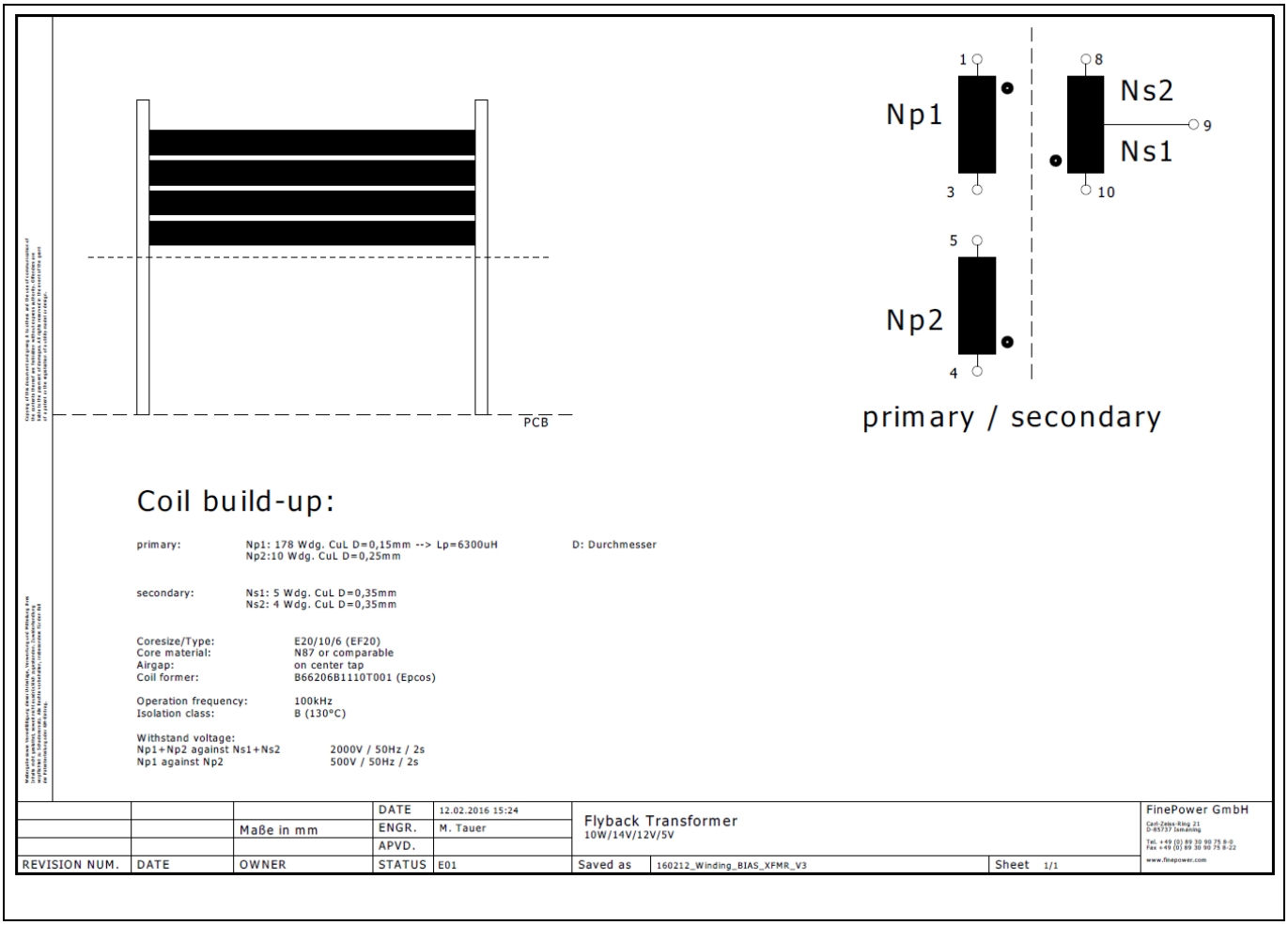



| Windings | Start | End | Wire | Turns | Layers | Method |
|---|---|---|---|---|---|---|
| N1 | 1,2,3 | 4,5,6 | 60x0.2mm Litz | 9 | 1 | Tight |

The inductor is produced by Infineon's trusted partners in the development and manufacturing of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY – http://www.kaschke.de/en/home/
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY – http://www.icetransformers.com/en/

### 3.5.3 Auxiliary transformer




The transformer is produced by Infineon's trusted partners in the development and manufacturing of magnetic components:

- **Kaschke Components GmbH** – Göttingen, GERMANY – http://www.kaschke.de/en/home/
- **ICE Transformers s.r.l.** – Loreto Aprutino (Pescara), ITALY – http://www.icetransformers.com/en/

# 4 Digital control features

The control of the 3 kW dual-phase LLC converter has been implemented using XMC4400, which is part of the XMC™ microcontroller family from Infineon Technologies. This family is based on an ARM® Cortex®-M4 core, and the main features were summarized in section 3.3.5. The following section introduces the main features of the implemented digital control as well as the resources necessary for proper implementation.

## 4.1 Resources and implementation concept

### 4.1.1 Resources (peripherals)

XMC4400 has been selected due to the complexity of the design, which requires a high number of peripherals as well as a high calculation power. By using the required peripherals for one of the LLC phases as an example, this section presents the necessary resources for the multi-phase LLC design.

Figure 17 depicts the available resources in the selected XMC4400 microcontroller. For a single LLC phase the following resources are used:

- Four timers for PWM generation of both HB and SR switches. XMC4400 includes two different timers (CCU4 and CCU8), which provide not only PWM outputs but a flexible and programmable signal-conditioning scheme thanks to the available interconnections with other peripherals. In the dual LLC two CCU4 and two CCU8 timers are used for each phase.
- Two Event Request Unit (ERU) slices for proper interconnection of the timers. The ERU is a versatile event detection and processing unit which increases the peripheral connectivity.
- One high resolution PWM (HRPWM) which includes a high resolution timer (HRC) and an analog Comparator with Slope Generation (CSG).
- Five ADC channels. These include the input and $V_{out}$ sensing, which are common for both phases, as well as output current, $I_{res}$ and temperature, which are measured for each phase.
- Apart from compare mode to generate PWM signals, CCU4 timers can be used in capture mode in order to acquire time between different events. Two CCU4 timers are used in capture mode for frequency and time acquisition.

Apart from these specific resources, other shared peripherals are required for proper operation of the application:

- One serial communication channel (USIC) is used for communication with the graphical user interface (GUI). The USIC configured in UART mode can be connected to a PC through a serial COM port. This channel is associated with two interrupts for receiving and transmitting the data.
- The XMC4400 processor has a 24-bit system timer (SysTick) which counts down to zero from a defined value. This special timer is used in the dual LLC for scheduling purposes to trigger a fixed frequency interrupt. The application SW is executed in this interrupt.
- Part of the Flash memory is utilized to store the converter parameters sent via GUI. XMC4400 provides up to 512 kB of Flash memory and therefore, no external EEPROM is necessary.

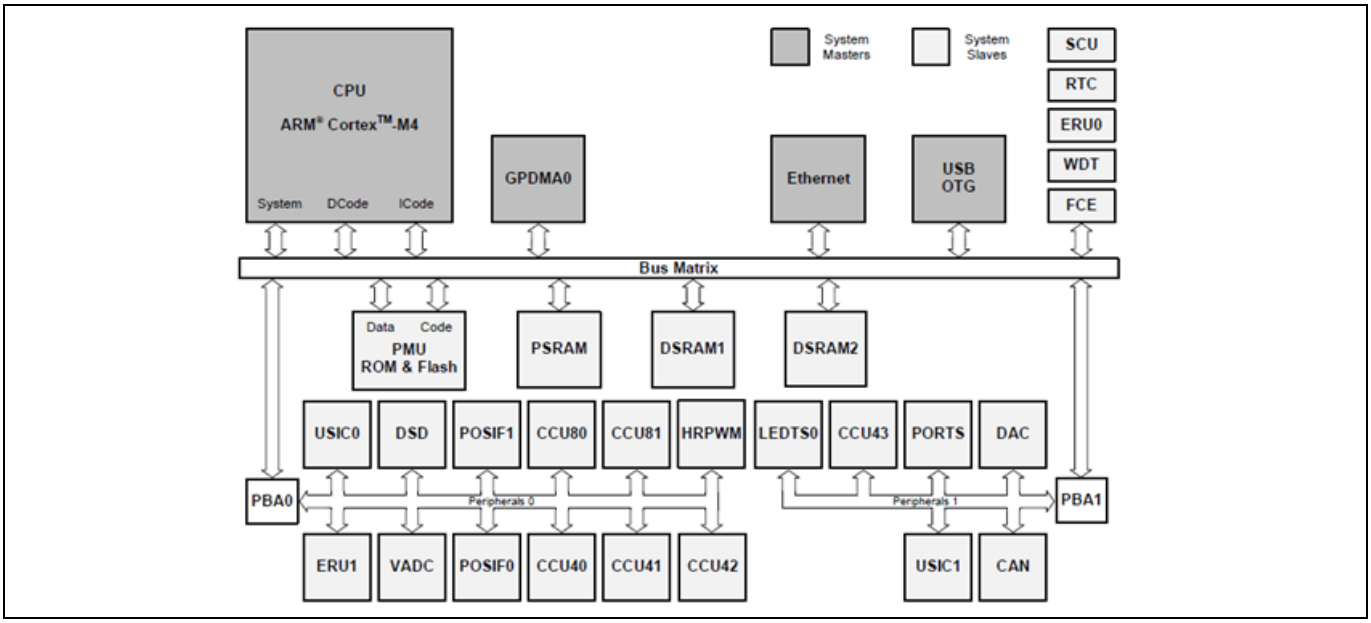



**Figure 19 XMC4400 system resources**

Including the previously mentioned resources, the complete list of resources is summarized in Table 1.

**Table 1 Peripherals used in the dual LLC control implementation in XMC4400**

| XMC Peripheral | Resource | used / available |
|---|---|---|
| CCU8 | timer | 6 / 8 |
| CCU4 | timer | 8 / 16 |
| VADC | channel/pin | 8 / 9 |
| USIC | channel | 1 / 4 |
| PORTS | pin | 33 / 44 |

### 4.1.2 Implementation concept

Besides the previously described peripherals, the implemented control algorithms are executed in a regular time base. The system timer (SysTick) sets this regular time base, thus fixing the sample rate as well as the loop execution. The main functionality of the multi-phase converter is implemented in the control interrupt routine, triggered by the system timer (Figure 20). This functionality includes the following processes:

- Output current limitation protection
- Capacitive mode protection
- Burst mode management
- PI controller
- Start sequence
- Phase shedding
- SR management
- Dead-time calculation
- SW ADC trigger of the control variables

### Digital control features

As shown in Figure 18, the PWM signal with 50% duty cycle is generated using a CCU8 timer. The flexibility of this peripheral in the XMC4000 series enables a synchronized trigger of the $I_{res}$ ADC measurement with the generated PWM signal.

In addition, the versatile ADC enables scheduling of different measurements by using different measurement groups with different triggers and priorities. In the selected implementation the $I_{res}$ is measured using the queue function triggered by the PWM. However, the rest of the channels are configured as background measurements with lower priority and are triggered by SW in the control interrupt.

Furthermore, the CCU8 timer can easily be connected to the HR channel of the HRPWM peripheral. This connection not only enables utilization of the 150 ps PWM resolution of this peripheral, but enables the update of the PWM dead time in a safe manner, as will be explained later.

More information about the highly configurable ADC and timer peripherals can be found in [14].

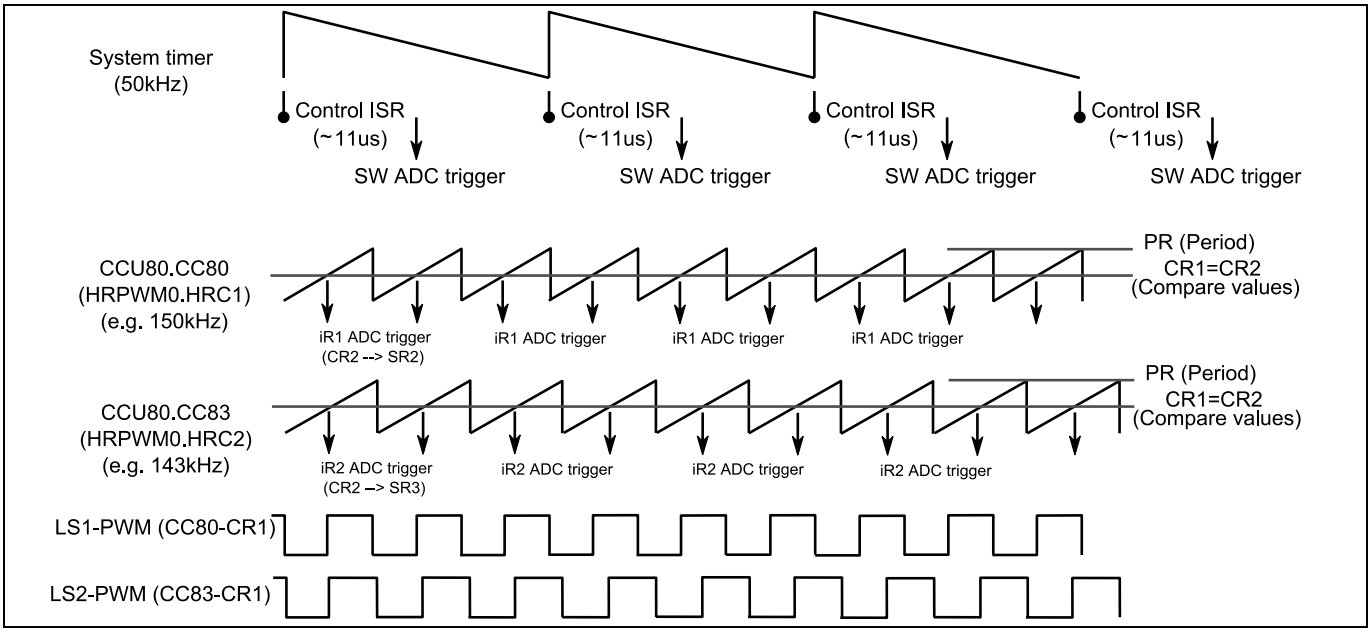



**Figure 20 Time diagram of the 3 kW dual-phase LLC converter digital control implementation**

As shown above, the selected implementation is based on a single interrupt with the highest priority. However, there are other tasks that are implemented in different background processes. Since the interrupt cannot be preempted by the lower-priority tasks, such as the background ones, these last ones are assessed in the remaining processing time between interrupts:

- State machine
- Fault management
- SR time calculation
- Compensator coefficients according to $C_{OSS}$ selection
- Power balance between phases
- Memory observer
- Communication with GUI
- Time counting

In the next sections the main functionality implemented in the 3 kW dual HB LLC converter will be explained in more detail.

## 4.2 Current sharing and phase shedding

In section 2.1.2 the concept of implemented current sharing was described. As already explained, both converter phases are controlled using related, but different, switching frequencies in order to balance the current between the phases. This difference in $F_{sw}$ can be observed in Figure 21 by the difference in phase of both resonant currents at different moments in time, for the same output power. In addition, the number of active phases is modified according to the load level, with the goal of achieving a flat efficiency across a wide load range.

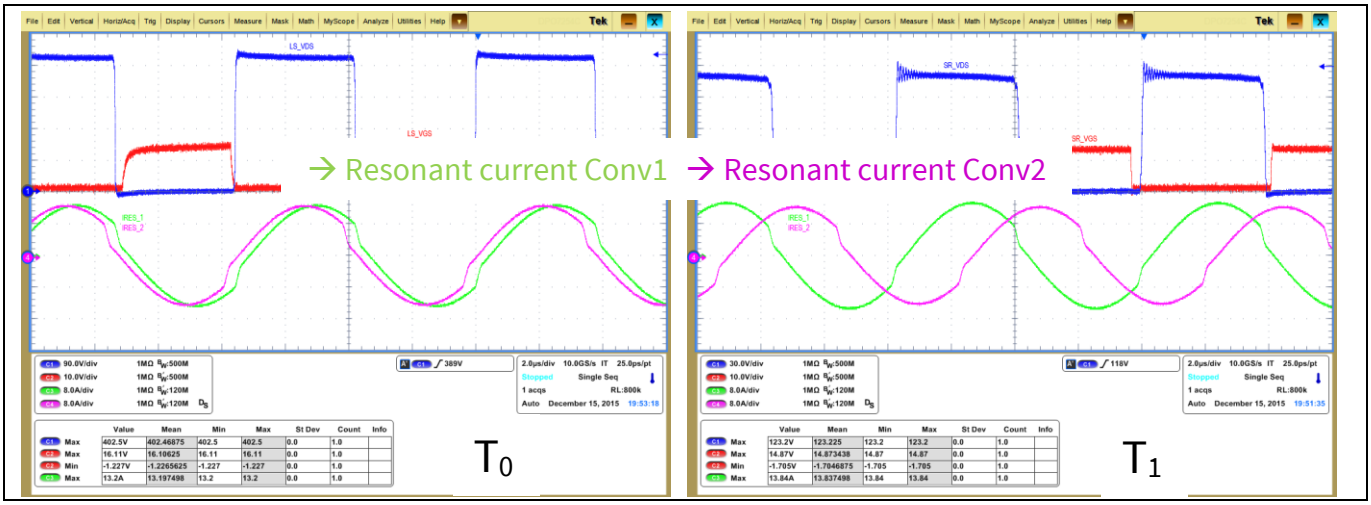



**Figure 21 Phase difference of phase 1 (green) and phase 2 (purple) resonant currents at the same power at two different moments in time**

The implemented current sharing and phase shedding introduced in Figure 8 is redrawn in Figure 22 to show the different blocks involved in the process: both LLC phases (Conv1 and Conv2), a PI controller to ensure $V_{out}$ regulation, and a current balancer that decides the $F_{sw}$ to be applied to each phase.

The PI controller is evaluated every control interrupt (50 kHz) according to the sensed $V_{out}$ and the required voltage target. This voltage target varies during soft-start, and it can have different steady-state values, according to the specifications presented in Section 3.1. The steady-state $V_{out}$ can be modified via the GUI.

The output of the PI controller, which is the necessary $F_{sw}$ to match the $V_{in}/V_{out}$ gain, is fed to a current balancer block, together with the output current measurements of each LLC converter.

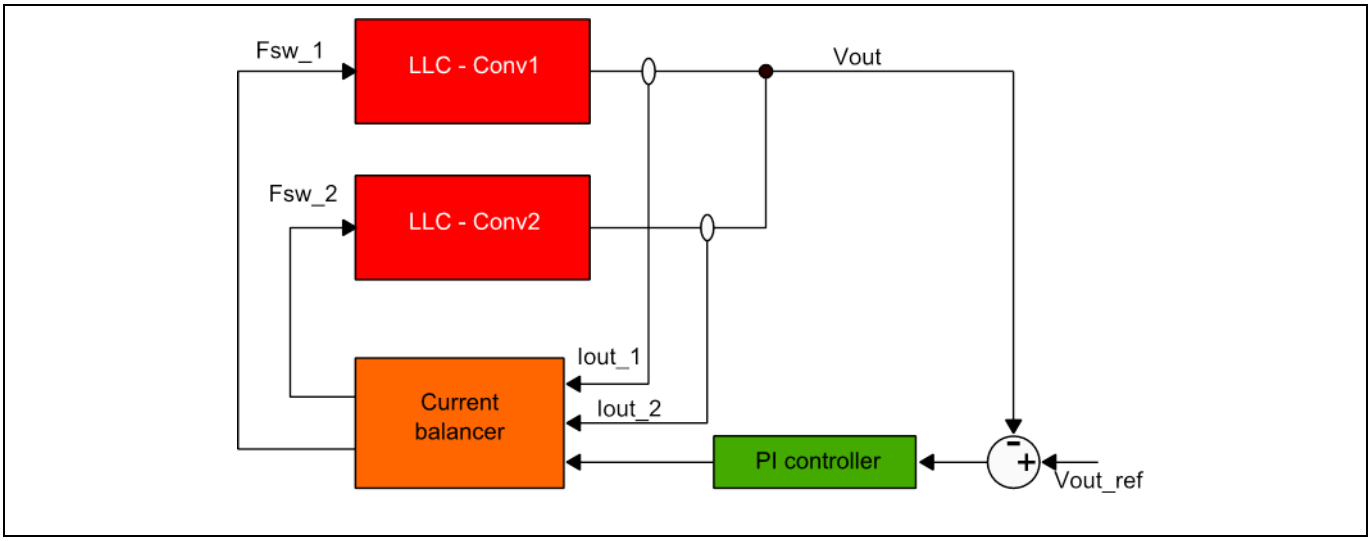



**Figure 22 Block diagram of the current-sharing and phase-shedding functionalities**

The current balancer uses this information to calculate the $F_{sw}$ of both LLC converters, considering not only the $V_{out}$ regulation but also a maximum current difference of 5 A between the phases. The balance mechanism is based on an intermediate variable, which is modified in an iterative manner, tracking the frequency calculated by the PI controller. The step of the iteration depends on the number of active phases as well as how far the balancer variable is from the output of the PI controller. This mechanism runs as a background process and corresponds to the slow control named as efficiency controller in Figure 8.

The previously presented variable to achieve current balance is slowly modified to guarantee steady-state current sharing and stability. However, a different mechanism is required to handle external perturbations with a fast response. The current balancer variable is therefore immediately modified (in the control service routine running at 50 kHz) when one of the following events is detected: current limitation (Section 4.4.1), load jump and dump, and capacitive mode detection (Section 4.3.2). These three mechanisms are included in the block named as dynamic control in Figure 7.

The efficiency controller, inside the current balancer, is also responsible for the phase-shedding functionality. In this case, the number of active phases is modified to achieve an efficiency curve that is as flat as possible. Two different thresholds separated by a certain hysteresis are defined to decide whether the second phase is enabled or disabled. The current thresholds are defined for the total output current and change according to the $V_{out}$ target, as shown in Figure 23.

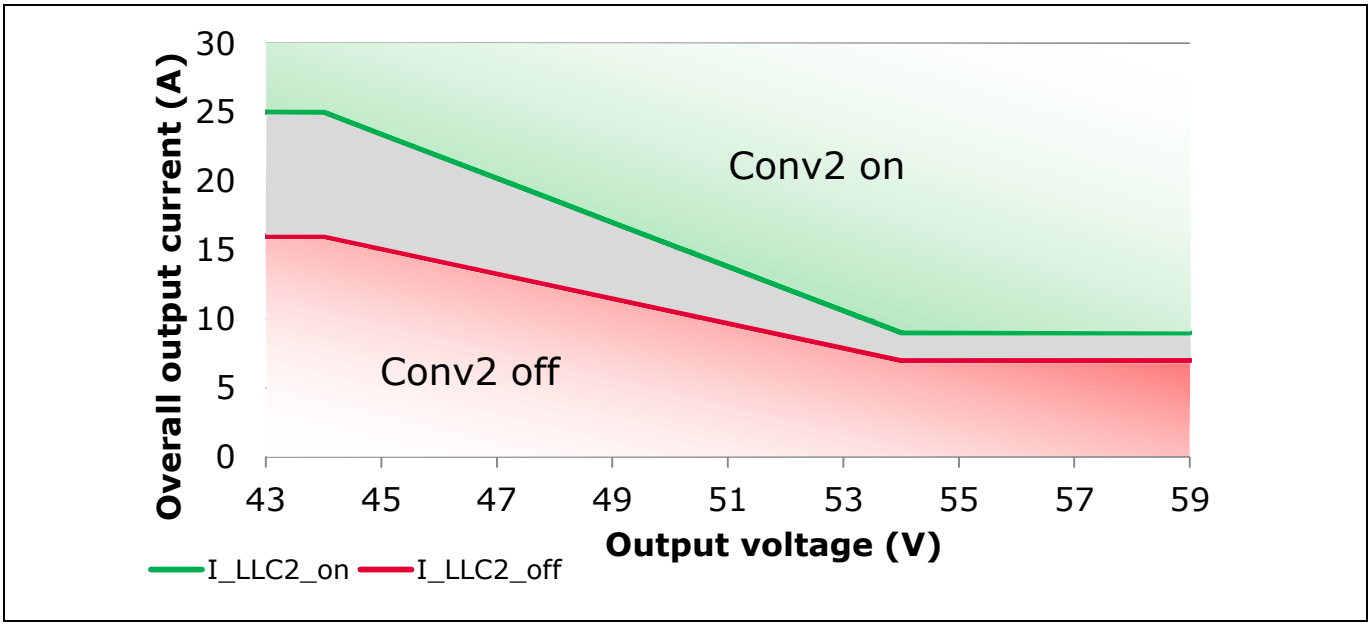
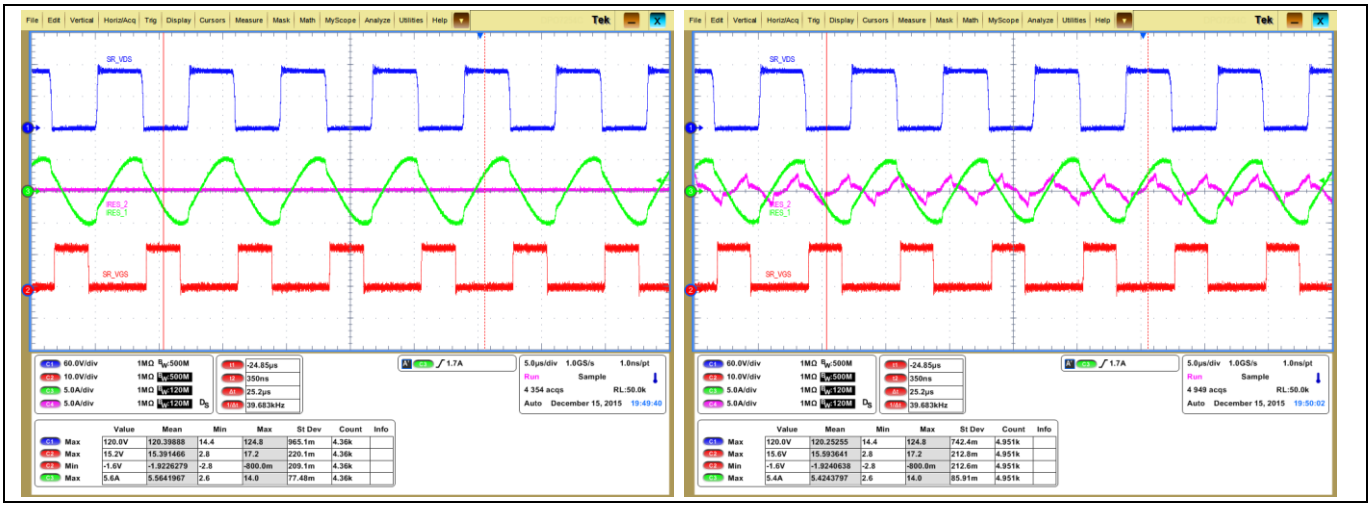



**Figure 23 LLC Conv2 shedding depends on overall output current thresholds for a given target voltage**

The presented current levels are applied in steady-state operation of the converter. A third threshold is implemented in order to enable Conv2 as soon as a positive load jump is detected, thus providing an adequate transient response. The enabling of Conv2 for a $V_{out}$ of 54 V, when a smooth load transition across the defined on-threshold is applied is shown in Figure 24. As can be seen, the applied load change is small, to change the phase 1 $F_{sw}$, but enough to start the operation of phase 2, which can be seen in the change of its resonant current.

It must be noted that the second stage operates only in the case that the first phase is active. In case Conv1 is turned off, e.g. in burst mode operation, Conv2 is automatically disabled and later enabled according to the actual current levels.



a) b)

**Figure 24 Resonant current of phase 2 (purple) for single-phase operation (a) and when phase 2 is enabled (b) after the current threshold is reached**

## 4.3 Hard-commutation prevention and capacitive mode detection

As shown in Section 2.2, reliability is a concern in SMPS. In LLC converters, hard-commutation is a typical failure mechanism under certain operating conditions. The dual LLC shown in this document implements two mechanisms to avoid hard commutation and capacitive mode operation respectively, as it was briefly outlined above. This section introduces the concept as well as the microcontroller implementation for both mechanisms.

### 4.3.1 Hard-commutation prevention

In order to avoid hard-commutation during start-up, or when resuming operation in burst mode, a special sequence is implemented for both phases of the 3 kW dual-phase LLC converter. The applied sequence is divided into four phases, as shown in Figure 25, which will be explained in more detail in this section.

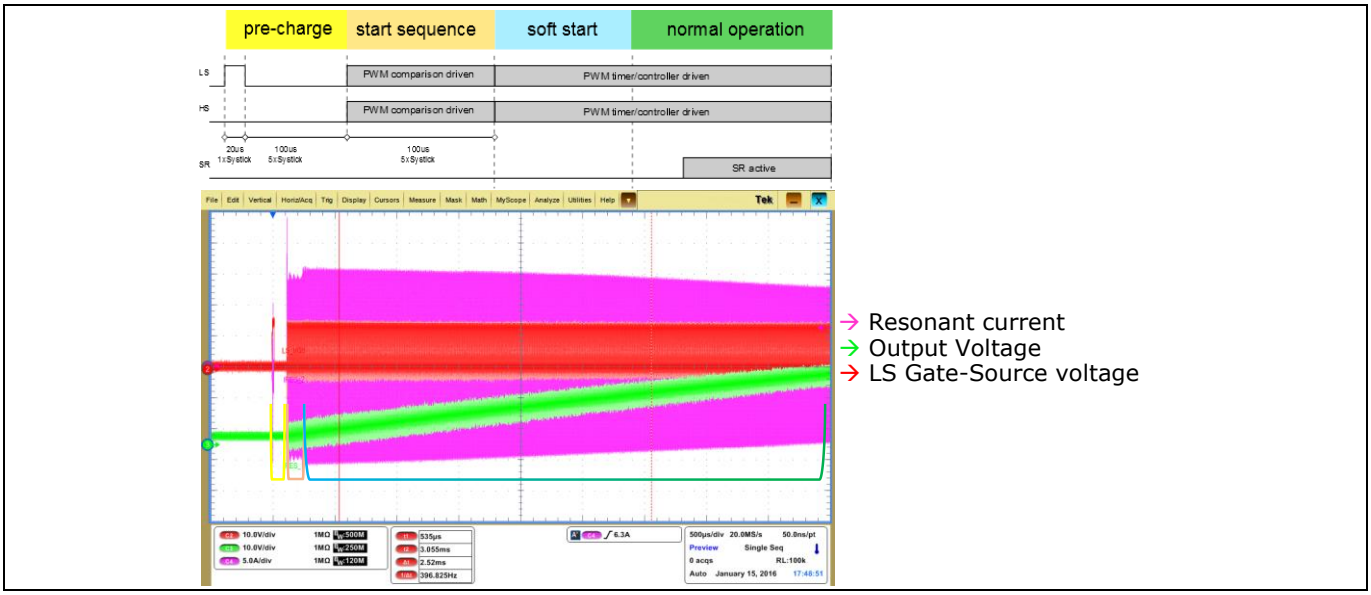



**Figure 25 Converter start-up with the applied four-phase sequence**

1. **Pre-charge:** The aim of this phase is to charge the driver bootstrap capacitor to apply the proper PWM sequence afterward. Therefore, before starting the converter a long pulse of 20 µs is applied to the LS switch while the HS is kept off (A). Afterward both switches are off for 100 µs (B). In this phase the SR are kept off. Figure 26 shows a scope capture of this phase during Conv1 start-up, together with the first pulses of the next phase in the applied sequence.

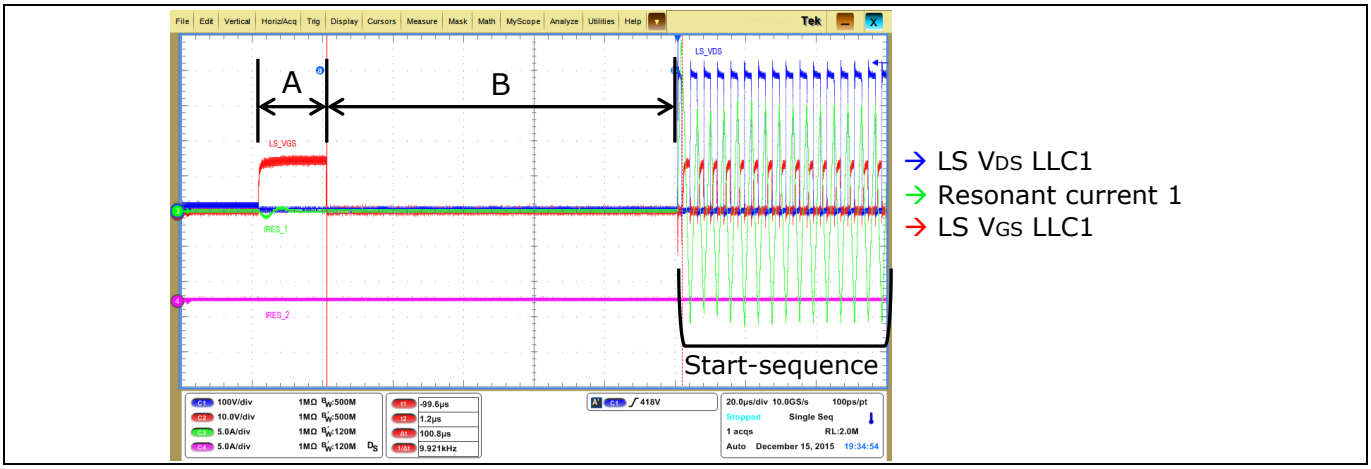



**Figure 26 Pre-charge phase scope capture [Ch1 = $L_{S_Vds1}$; Ch2 = $L_{S_Vgs1}$; Ch3 = $I_{res1}$; Ch4 = $I_{res2}$]**

2. **Start-sequence:** With the driver bootstrap capacitor properly charged, the converter operation can be started as shown in Figure 24. In order to avoid hard commutation during the first cycles of the converter start-up, the PWM is driven by the comparison of the $I_{res}$ with zero. This allows for delaying the change between LS and HS (and vice-versa) after the current zero crossing. As a consequence the change in the current polarity is guaranteed and hard commutation avoided as shown in Figure 25. This phase is applied for 100 us, and the SR switches are kept off.

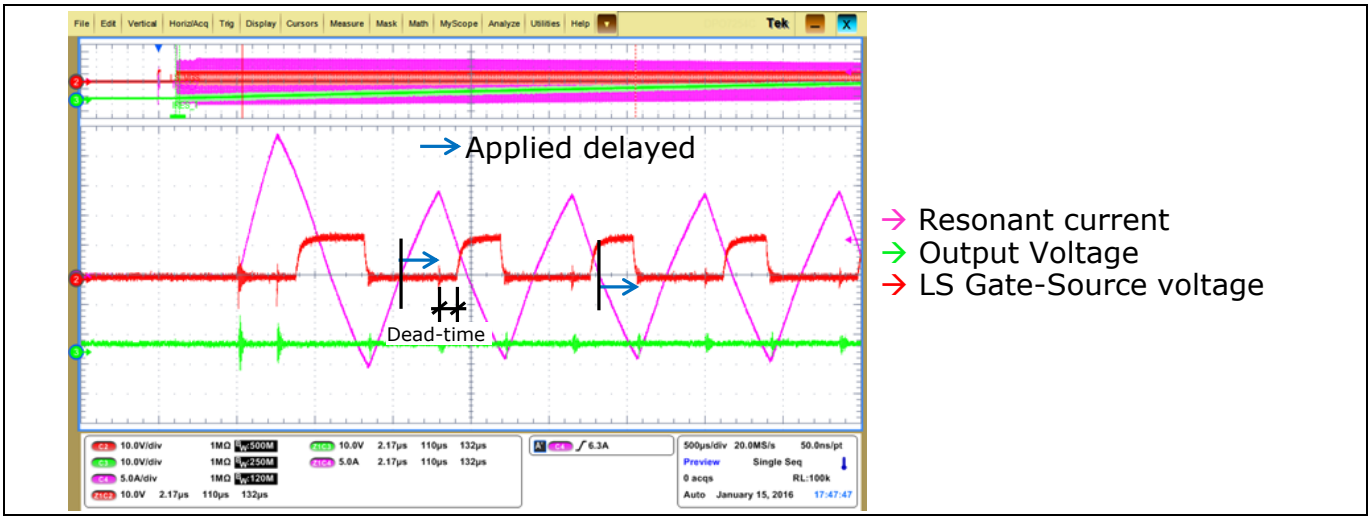



**Figure 27 LS-HS driving signal change is applied with a delay after the $I_{res}$ crosses zero to guarantee current polarity change and avoid hard commutation**

1) and 4) **Soft-start and normal operation:** During the previous phase the time between two consecutive crosses of zero is captured cycle-by-cycle using a CCU4 unit in capture mode. The acquired time is used as the period of another timer, thus generating a timer replica. After the 100 us comparison-driven phase the timer replica is used to drive the PWM, ensuring a smooth transition (Figure 28). At the same moment the $V_{out}$ is sensed and ramped to achieve the target voltage (soft-start). When the target voltage is achieved (normal operation) SR is managed according to certain conditions, which will be explained elsewhere.

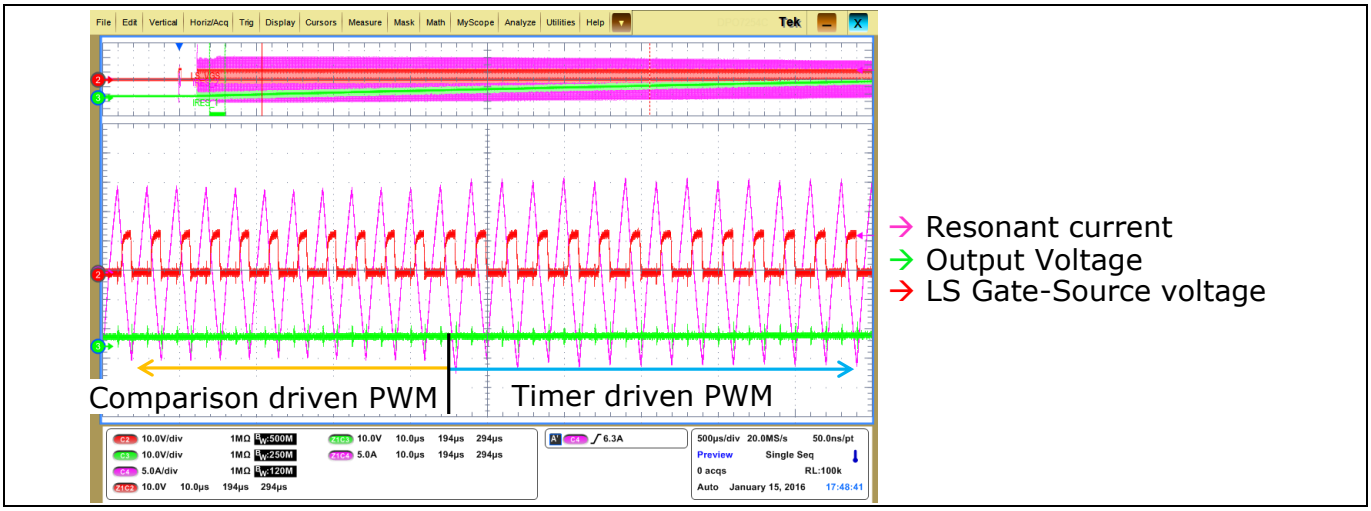



**Figure 28 Smooth transition between comparison-driven and timer-driven PWM operation due to the implemented timer replica**

### 4.3.2 Capacitive mode detection and prevention

In capacitive load mode operation the resonant current leads the voltage in the mid-point of the HB. Therefore, the operation in this mode, or the tendency to move from inductive to capacitive mode, can be monitored by knowing the phase difference between the previously mentioned current and voltage.

In the design shown here, for each converter, this phase information is obtained by capturing the time between the PWM output edge and the corresponding zero crossing detection of the resonant current (Figure 29). In order to increase the robustness of the implementation, the previous PWM edge to the selected zero crossing is used for the time captured, as shown in Figure 27. This modifaction enables measurement of the negative phase for fast capacitive mode detection. With the captured time information, the actual phase difference can be calculated by SW, since the switching period is known.

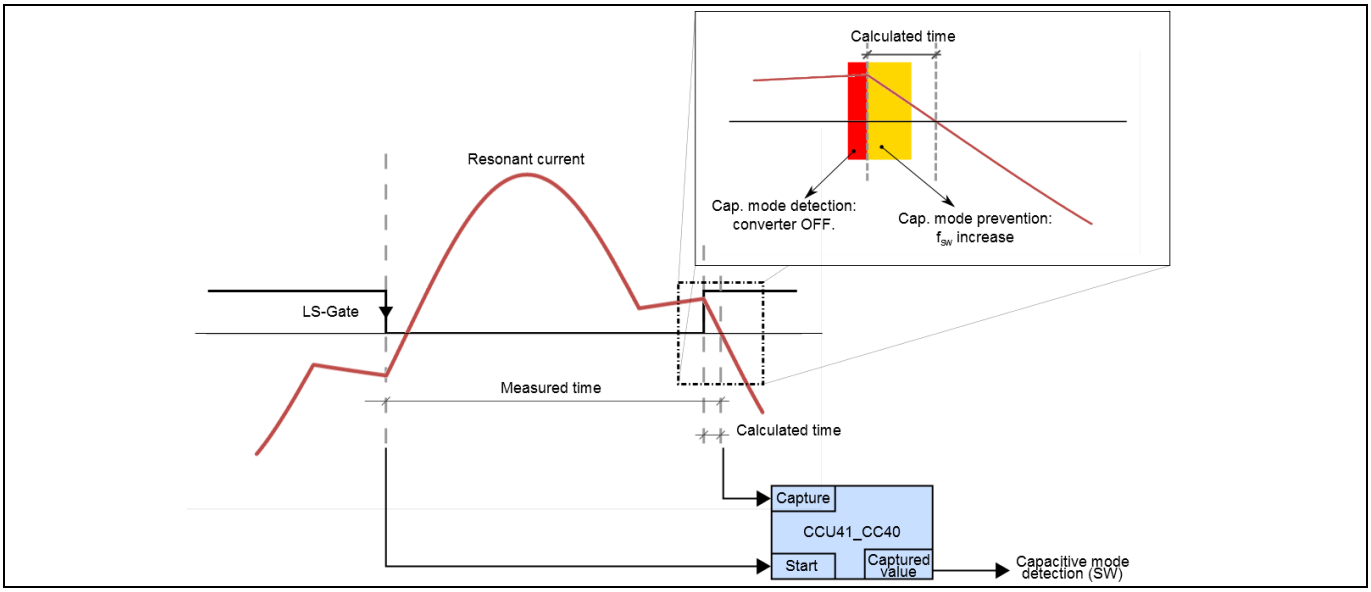



**Figure 29 CCU4 timer in capture mode to acquire the phase difference between voltage and current and capacitive mode prevention and detection phase thresholds**

With this phase difference information two different protection mechanisms can be triggered: capacitive mode prevention and capacitive mode detection.

- When the captured phase difference decreases toward zero under a certain defined threshold, the prevention algorithm is activated. This prevention consists of increasing the $F_{sw}$ by decreasing the $V_{out}$ target. The implemented algorithm can shut down the converter if, after several successive tries at increasing the $F_{sw}$, the phase difference remains under the defined threshold.
- The second mechanism is capacitive mode detection. Capacitive mode is detected if the captured threshold is zero or negative for two consecutive sampling periods. As a result of detecting capacitive mode the converter is immediately turned off. The latching behavior of the protections can be selected via the GUI, as explained later in this document.

## 4.4 Protections

Two different levels of protections have been implemented in the microcontroller, depending on the variable being monitored. Those that require fast reaction (linked to the input and output current) are evaluated in the interrupt service routine associated to the control loop. The other variables are monitored in the background process with different filter times, as explained below.

The latching behavior of the implemented protections can be controlled using the GUI, with the exception of the over-temperature protection, which is always the latching type. By default the protections are configured to be non-latching, and the converter will try to restart 2 s after the fault has been detected.

### 4.4.1 Over-current protection

Different limits and algorithms have been implemented for each phase of the dual LLC converter regarding output current (Figure 30). A first limit is set to distinguish between normal operation and over-current conditions. If the sensed output current is over this threshold, either current limitation or Over Current Protection (OCP) mechanisms are applied.

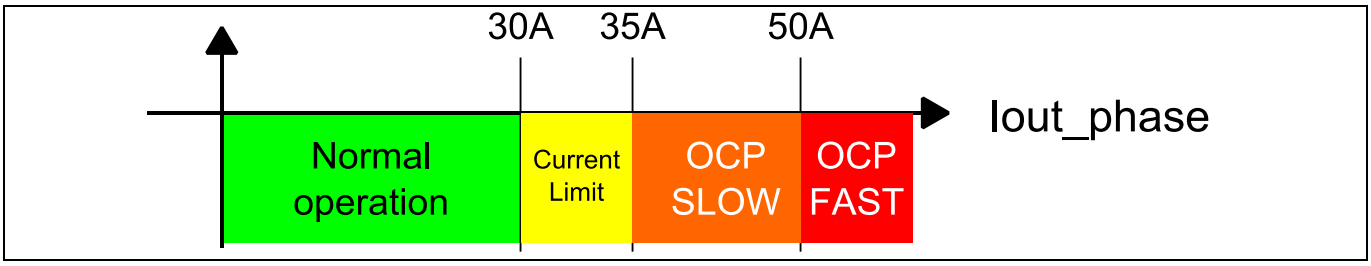



**Figure 30 Output current monitoring limits**

For the fastest current protection, OCP FAST in Figure 30, the sensed current is compared with the highest of the defined thresholds (50 A). The comparison is assessed every interrupt cycle (20 µs) and it is active after the soft-start phase of the starting sequence is completed.

A second level of OCP is defined with an intermediate threshold (35 A). In this case the protection is triggered if the sensed current remains over this value (OCP SLOW in Figure 30) during 40 ms.

If the sensed current is not reaching the OCP levels but is over the normal operation range, the current limit mechanism is triggered (Figure 31). Current limitation is applied via the $V_{out}$ target reduction, thus limititing the $F_{sw}$. Different scenarios are possible in this situation depending on the number of active phases:

- If only phase 1 is enabled, the current limitation is obviously applied based on the output current of that phase.
- In case both phases are enabled, the $V_{out}$ target reduction is applied considering only the output current of phase 2.
- Furthermore, if both phases are active and current over the 30 A threshold is detected in phase 1, the current balance is modified to increase the current provided by phase 2.

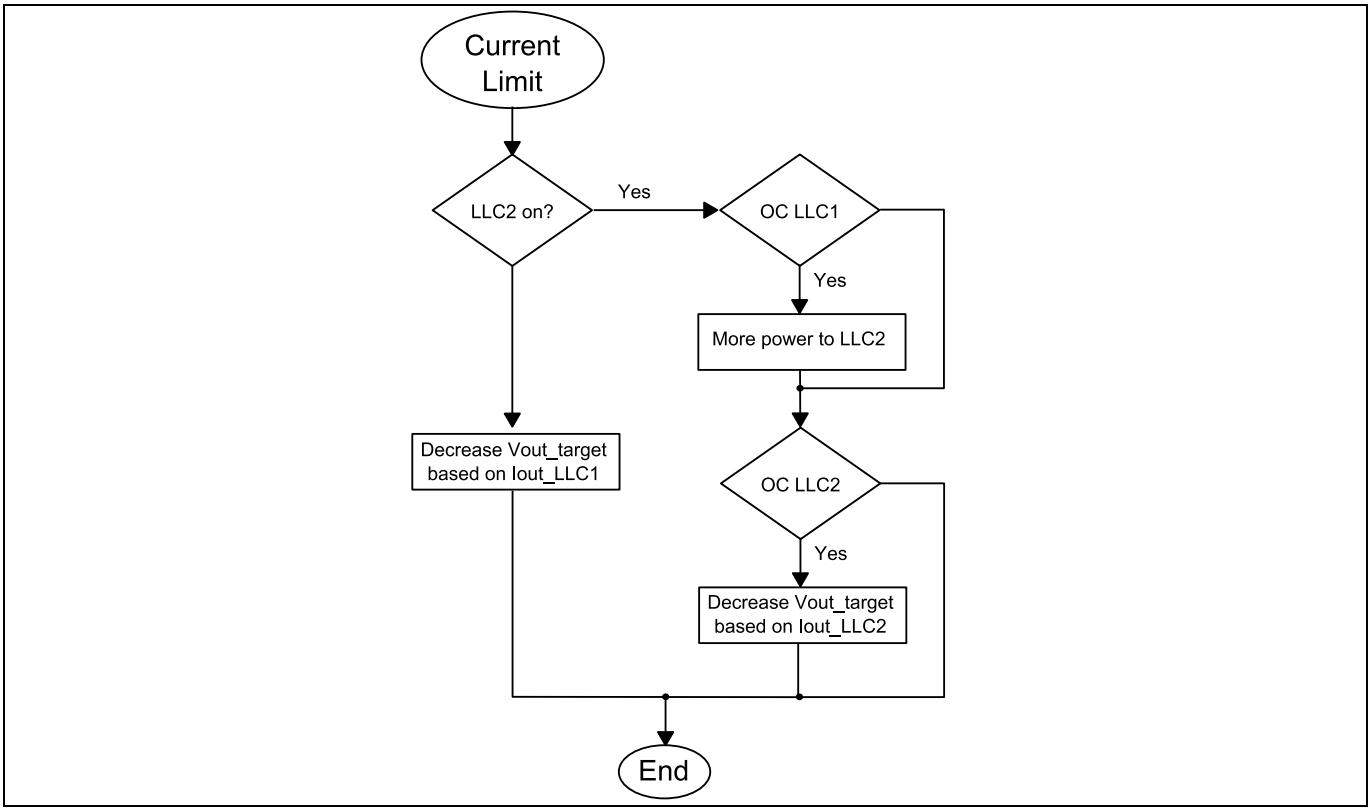



**Figure 31 Flow diagram of the current limit algorithm**

For any of the previously described current limitation scenarios, a fault is triggered if the current remains over the lowest threshold (30 A) during 2 s.

Besides the output current protections mentioned, there is an input OCP based on the $I_{res}$ measurement. Unlike the other sensed variables in the system, the $I_{res}$ ADC measurement is synchronized with the PWM of each phase (Figure 20). Therefore, accurate information of the $I_{res}$ value of each phase is obtained. This information is used to detect either over-current or capacitive mode operation, by means of a comparison with a fixed current threshold.

### 4.4.2 Input and output voltage monitoring

Both $V_{in}$ and $V_{out}$ are constantly monitored during operation of the dual LLC. In the case of the $V_{out}$, a fault is set when the sensed and filtered value is above a defined level. This limit can be configured using the GUI and is set to 62 V by default. Setting the fault implies that the converter turns off. The resumption of operation depends on the selected latching behavior in the user interface, as explained previously.

Regarding the $V_{in}$, both the upper and lower limits are defined. If the filtered sensed $V_{in}$ is outside the defined range the converter remains off. However, the converter is not latched and the operation resumes when the $V_{in}$ is inside the range. The minimum and maximum limits for this protection are fixed to 345 V and 415 V respectively, and cannot be modified via the user interface.

### 4.4.3 Other protections

Apart from the current and voltage protections for both input and output variables, other protections have been implemented in the presented converter.

Using the $V_{out}$ and output current measurements, the output power of each converter can be calculated. If the total output power is higher than a defined threshold, a fault is triggered and the converter is turned off. The limit cannot be modified and it is set by default to 3.2 kW. The same fault is reported in the user interface if the current limitation algorithm is not able to reduce the output current after 2 s.

An open-loop operation protection has also been implemented in the dual LLC converter. In open-loop operation, the $V_{out}$ FB is lost and the controller will try to increase the $V_{out}$ by reducing the $F_{sw}$. Therefore, this condition is detected if both phases are operating at minimum frequency for 1 ms, triggering the corresponding fault.

The last of the protections implemented is temperature protection for each phase of the converter. The temperature of each phase is sensed using NTCs coupled to the main transformer, and this information is fed to the microcontroller. According to the sensed temperature the fan is turned on (over 45°C) and off (under 35°C). Furthermore, a protection is triggered if the sensed temperature is over 80°C. This protection is always the latching type, and it cannot be modified using the GUI, thus a power reset of the converter is required.

## 4.5 Burst mode and SR management

In very light load or no-load conditions, burst mode is a common choice to maintain ZVS operation and solve regulation problems [8]. In the implementation shown, burst mode operation is triggered according to the $V_{out}$ level and the frequency of operation. An OV of 750 mV will start burst mode operation if the converter is operating at maximum frequency. Furthermore, if a 2.5 V OV is detected, regardless of the $F_{sw}$, the converter is turned off and burst mode operation is started. The following table summarizes the conditions that trigger burst mode operation.

**Table 2 Burst mode trigger conditions in the 3 kW dual LLC converter**

| Overvoltage | Swtiching frequency | Burst mode |
|---|---|---|
| > 750mV | max. freq. | YES |
| | < max. freq. | NO |
| > 2.5V | Not considered | YES |

Figure 32 (left) shows the primary-side waveforms of Conv1 during burst mode operation. It must be noted that burst mode operation is triggered in light-load operation and only Conv1 is enabled. The converter operation is resumed during burst mode when the $V_{out}$ target is reached again. In this condition, the starting sequence presented in section 4.3.1 is implemented to avoid hard-commutation, as shown in Figure 32 (right).

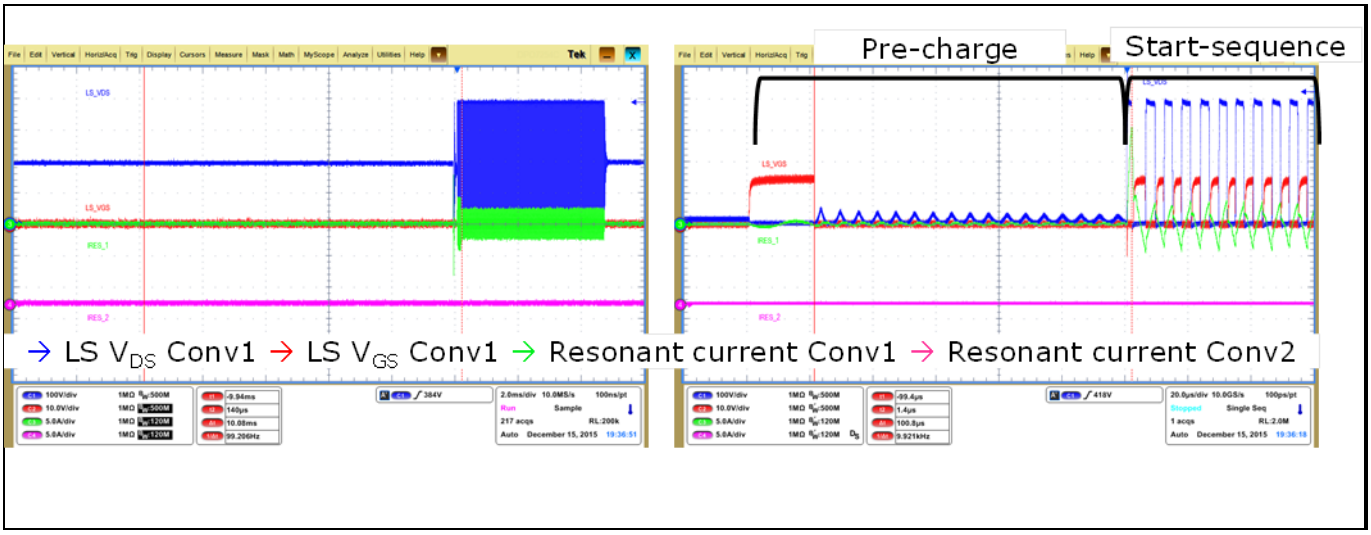



**Figure 32 Burst mode operation of the dual-phase LLC converter (left) and detail of the starting sequence during burst mode (right)**

SR management is applied to both phases independently. If burst mode operation is triggered, the synchronuous rectifiers (SR) are turned off to avoid reverse power flow and possible capacitive mode operation. Furthermore, SR switches are turned off for the same reason if a load jump is detected, as mentioned in Section 2.2. These conditions together with steady-state operating conditions to disable the SR switches are summarized in the following tables.

**Table 3 Synchronous rectifiers off conditions**

| OFF conditions | |
|---|---|
| OR | Iout_phase < 4A |
| | I resonant > 9.25A |
| | Vout < 42V |
| | Load change > 8A |
| Burst mode | |

Previously the off conditions were presented. On the other hand, SR switches for each phase are allowed to be turned according to the conditions present. When SR is enabled a soft-start of the on-time is applied to enable a smooth gain transition in the converter operation.

**Table 4 Synchronous rectifiers on conditions**

| SR ON conditions | |
|---|---|
| AND | Iout_phase > 4.5A |
| | I resonant < 9A |
| | Vout > 43V |
| | Load change < 8A |

## 4.6 Adaptive dead time

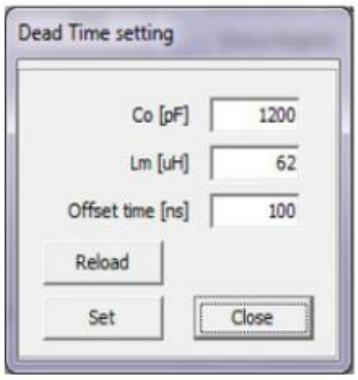
In order to maintain proper ZVS operation for different load and line conditions, a variable dead time between the driving signals of the HB is necessary. For a given design ($L_m$) and a given switch (time-related $C_{oss}$) the necessary dead time for a specific operation frequency can be calculated based on the following equation:

$$t_{DT}[ns] = DT_offset + 2 \cdot \sqrt{2} \cdot \pi^2 \cdot C_{oss} \cdot L_m \cdot f_{sw}$$

This equation is implemented in the dual HB LLC SW. Therefore, the proper dead time for the operating $F_{sw}$ of each phase is calculated. This calculation is done every control interrupt cycle (20 µs), according to the new calculated $F_{sw}$.

The required parameters can be provided through the GUI. Figure 33 shows the window of the GUI where the necessary parameters for the dead-time calculation can be provided. As an example of the required capacitance value, the time-related $C_{oss}$ of two CoolMOS™ transitors extracted from the available online datasheet are presented. If different CoolMOS™ transistors from different generations are used, it might be necessary to adjust the dead time. Therefore, a variable offset can be modified using the GUI for more precise adjustment.

The HRPWM peripheral included in the XMC™ enables safe modification of the dead time during operation. This safe update is possible due to the shadow transfer mechanism for the dead time included in the HRC of the HRPWM [14].




IPW60R031CFD7:

| | | | | | | |
|---|---|---|---|---|---|---|
| Effective output capacitance, time related[3] | $C_{o(tr)}$ | - | 2101 | - | pF | $I_D$=constant, $V_{GS}$=0V, $V_{DS}$=0...400V |

**Figure 33 GUI window to provide the necessary parameters for adaptive dead-time calculation for IPW60R031CFD7 CoolMOS™ transistor extracted from the datasheet**

## 4.7 Loop compensation parameters

As mentioned in Section 2.3, the total amount of output capacitance in the PSU is affected by the total capacitance present outside the unit. The total amount of capacitance seen by the PSU influences the loop stability and, therefore, the response of the unit to load and line jumps as well as any other external perturbance. Through the user interface developed for this dual-phase LLC converter, three different capacitors can be selected according to the output capacitor mounted by the user.

The three selectable capacitor values (4 mF, 6 mF and 8 mF) correspond to three sets of integral and proportional gains for the implemented PI controller in the voltage loop. The adequate set of integral and proportional gains is selected before the converter starts in accordance with the selected output capacitor in the user interface.

## 4.8 Graphical User Interface (GUI)

The GUI is a key part of our design concept, with the goal of enabling engineer interaction with the 3 kW dual-phase LLC during its evaluation on the bench. The main features of it were outlined in Section 2.3.

The physical aspects of the GUI are shown below – four main blocks can be seen:

- Setting and control: set the desired values for electrical parameters, converter operation and protections
- Measured values: measure the most relevant voltages, currents and temperatures
- Status register: short description of the converter operating conditions
- Fault register: flags showing the type of detected malfunction in case of forced shut-down

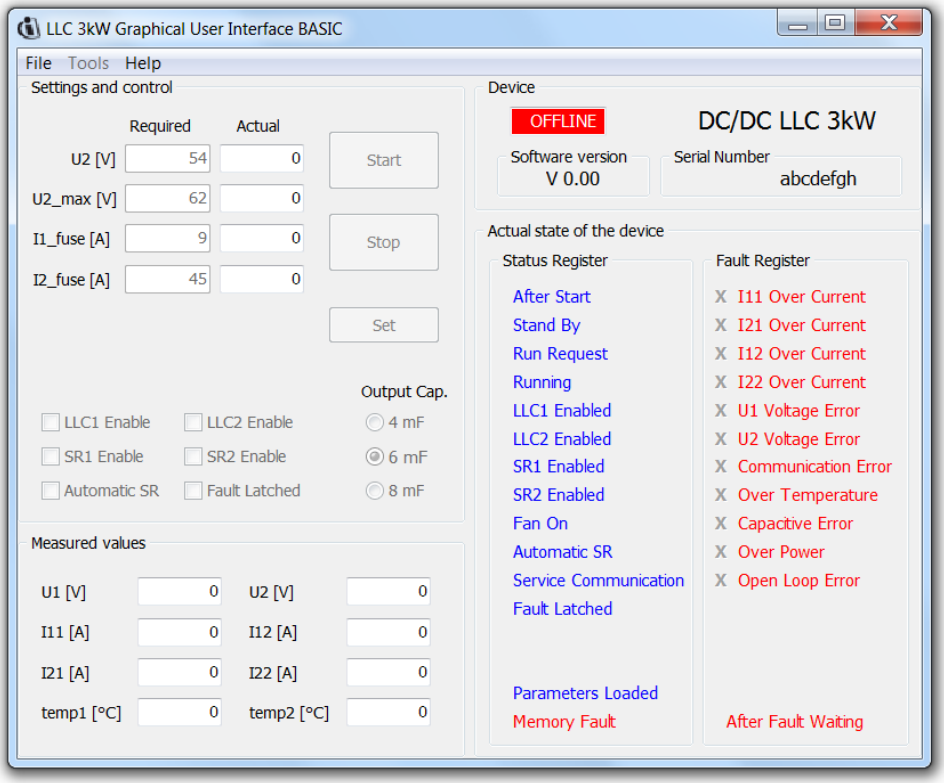



**Figure 34 LLC 3 kW Graphical User Interface (GUI)**

The benefits are evident: the GUI is an intuitive and user-friendly tool, even enabling changing the mode of operation of the converter without the need to modify any lines of code. It also provides real-time information on the status of the board, assuring constant monitoring, including in the case of shut-down due to the triggering of various protections.

By clicking on the icon below, the reader can find a detailed step-by-step guide to getting started with the GUI.

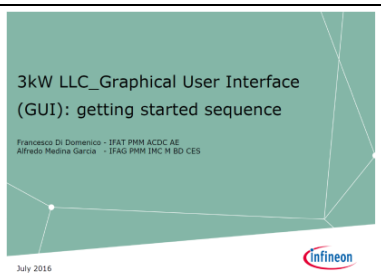



**Figure 35 3 kW LLC GUI – getting started**

# 5 Performance evaluation

This section provides an overview of the general operation and perfomance of the 3 kW dual-phase LLC.

The results were achieved on the primary side of both phases of the 600 V CoolMOS™ CFD7 in the TO-247 package (IPW60R031CFD7).

## 5.1 Waveforms captured in significant operation modes

The following figures show some of the most significant operation modes of the 3 kW dual-phase LLC.

Figures 36–38 illustrate the shape of the primary resonant tank and the gate and drain voltages measured on the low side (LS) MOSFET of Conv1. The unsynchronized switching frequencies of the two converters can be easily seen from the resonant current waveforms. The reduced peaks on the $V_{DS}$ and $V_{GS}$ demonstrate the accurate Infineon driving scheme and layout, which get the best performance out of the latest 600 V CoolMOS™ CFD7 technology. Special care must be taken in the selection of the gate resistances located in the turn-on and turn-off path of the HB MOSFETs: the choice is normally a trade-off between the efficiency target (especially related to switching losses) and reliability topics (mostly related to drain-source voltage de-rating guidelines). In our case, the selection of $R_{G,on}$ = 47 Ω and $R_{G,off}$ = 1 Ω enabled us to combine excellent ZVS behavior and reduced switching losses with very limited stress on the device. Bear in mind that the value of these resistances must be selected case by case, according to the PCB layout, the control applied during the start-up sequence, or output short-circuit protection for example.

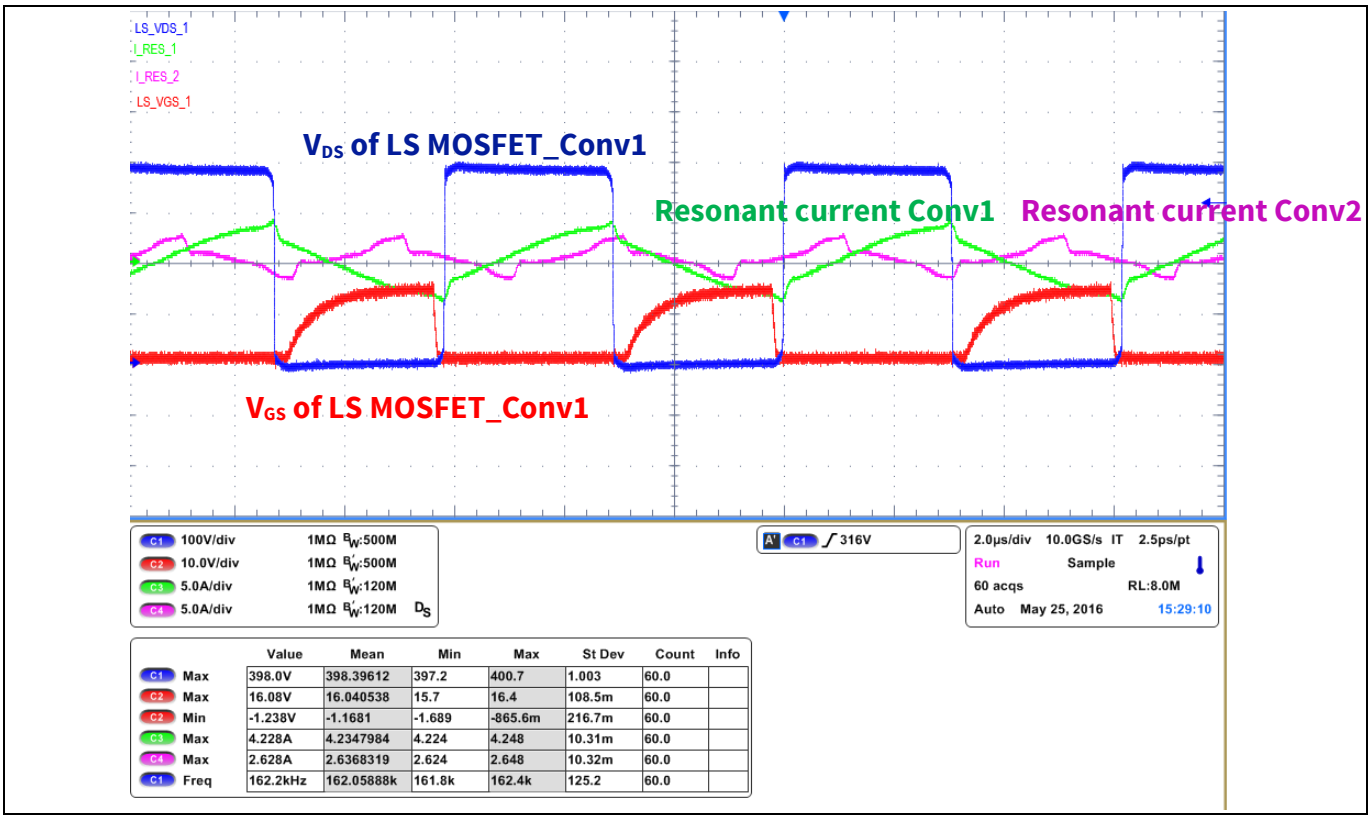
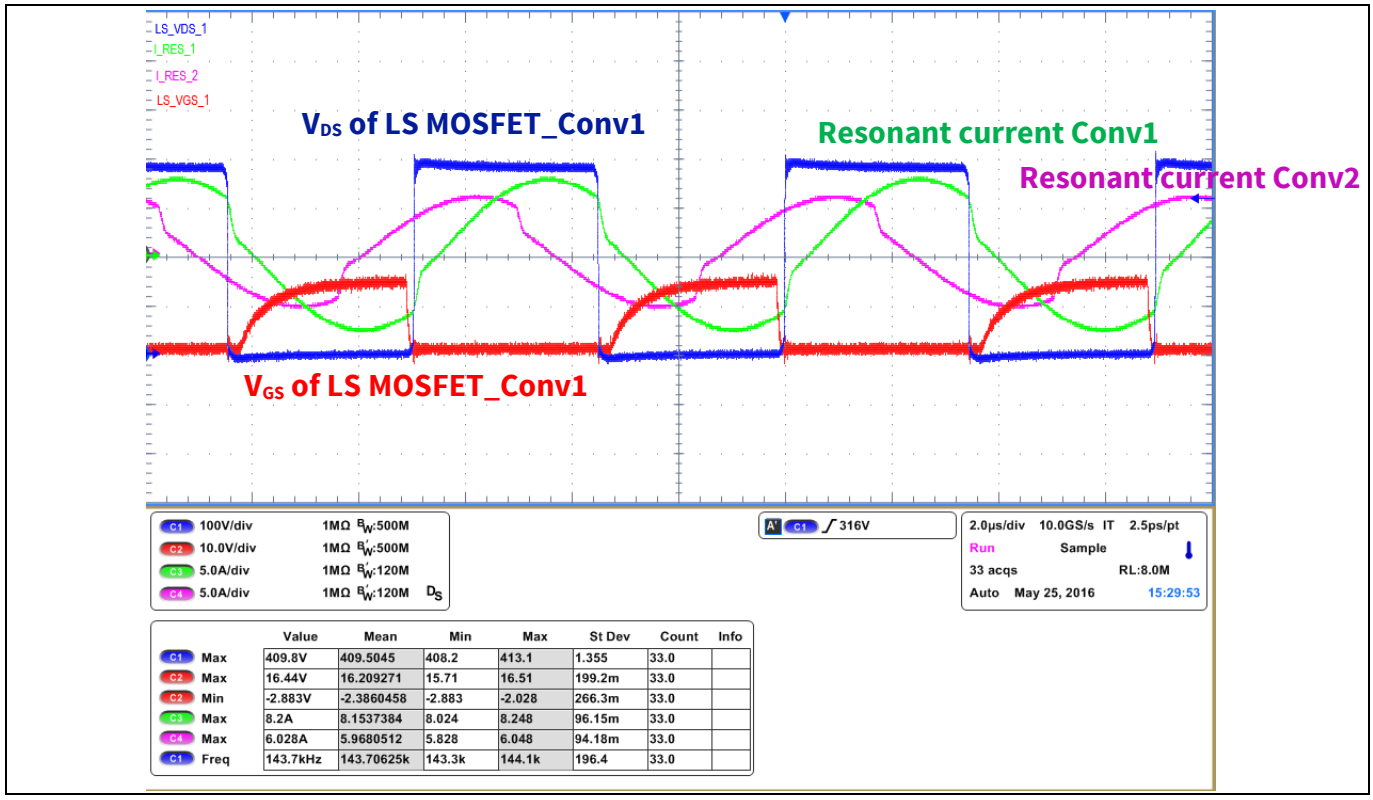
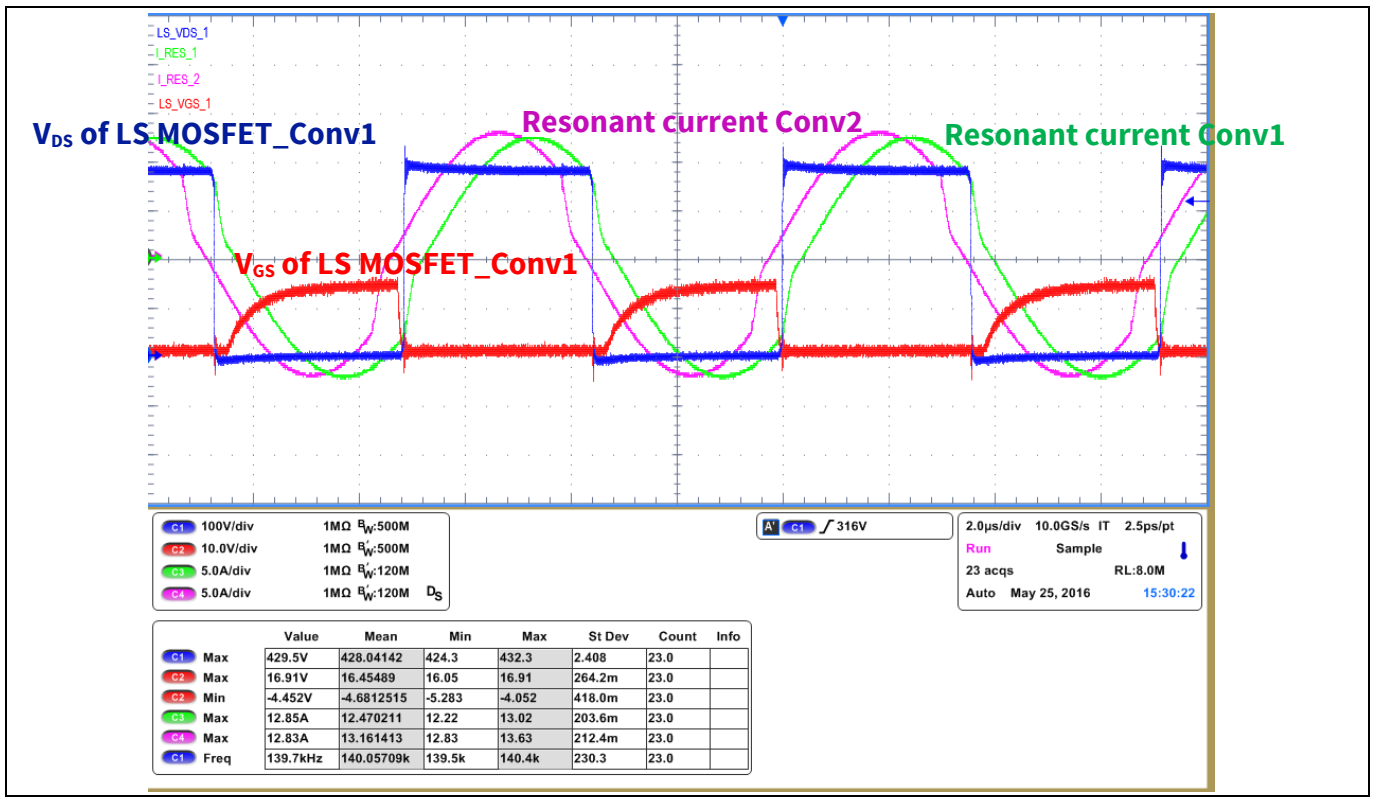



**Figure 36 Resonant currents: $V_{GS}$ and $V_{DS}$ on the LS MOSFET (Conv1) at 10% load**




| | Value | Mean | Min | Max | St Dev | Count | Info |
|---|---|---|---|---|---|---|---|
| C1 Max | 409.8V | 409.5045 | 408.2 | 413.1 | 1.355 | 33.0 | |
| C2 Max | 16.44V | 16.209271 | 15.71 | 16.51 | 199.2m | 33.0 | |
| C2 Min | -2.883V | -2.3860458 | -2.883 | -2.028 | 266.3m | 33.0 | |
| C3 Max | 8.2A | 8.1537384 | 8.024 | 8.248 | 96.15m | 33.0 | |
| C4 Max | 6.028A | 5.9680512 | 5.828 | 6.048 | 94.18m | 33.0 | |
| C1 Freq | 143.7kHz | 143.70625k | 143.3k | 144.1k | 196.4 | 33.0 | |

**Figure 37 Resonant currents: $V_{GS}$ and $V_{DS}$ on the LS MOSFET (Conv1) at 50% load**




| | Value | Mean | Min | Max | St Dev | Count | Info |
|---|---|---|---|---|---|---|---|
| C1 Max | 429.5V | 428.04142 | 424.3 | 432.3 | 2.408 | 23.0 | |
| C2 Max | 16.91V | 16.45489 | 16.05 | 16.91 | 264.2m | 23.0 | |
| C2 Min | -4.452V | -4.6812515 | -5.283 | -4.052 | 418.0m | 23.0 | |
| C3 Max | 12.85A | 12.470211 | 12.22 | 13.02 | 203.6m | 23.0 | |
| C4 Max | 12.83A | 13.161413 | 12.83 | 13.63 | 212.4m | 23.0 | |
| C1 Freq | 139.7kHz | 140.05709k | 139.5k | 140.4k | 230.3 | 23.0 | |

**Figure 38 Resonant currents: $V_{GS}$ and $V_{DS}$ on the LS MOSFET (Conv1) at 100% load**

Figures 39–40 focus on the ZVS behavior, which is achieved even at very light load.

## Performance evaluation

You can easily see the achievement of ZVS from the absence of the Miller Plateau in the $V_{GS}$ waveforms, which is a sign that the $V_{DS}$ returns to zero before the device is turned on. This will obviously minimize the device switching losses, which will only affect the turn-off transition, thus maximizing the converter's efficiency especially at light load, where the switching losses are dominant.

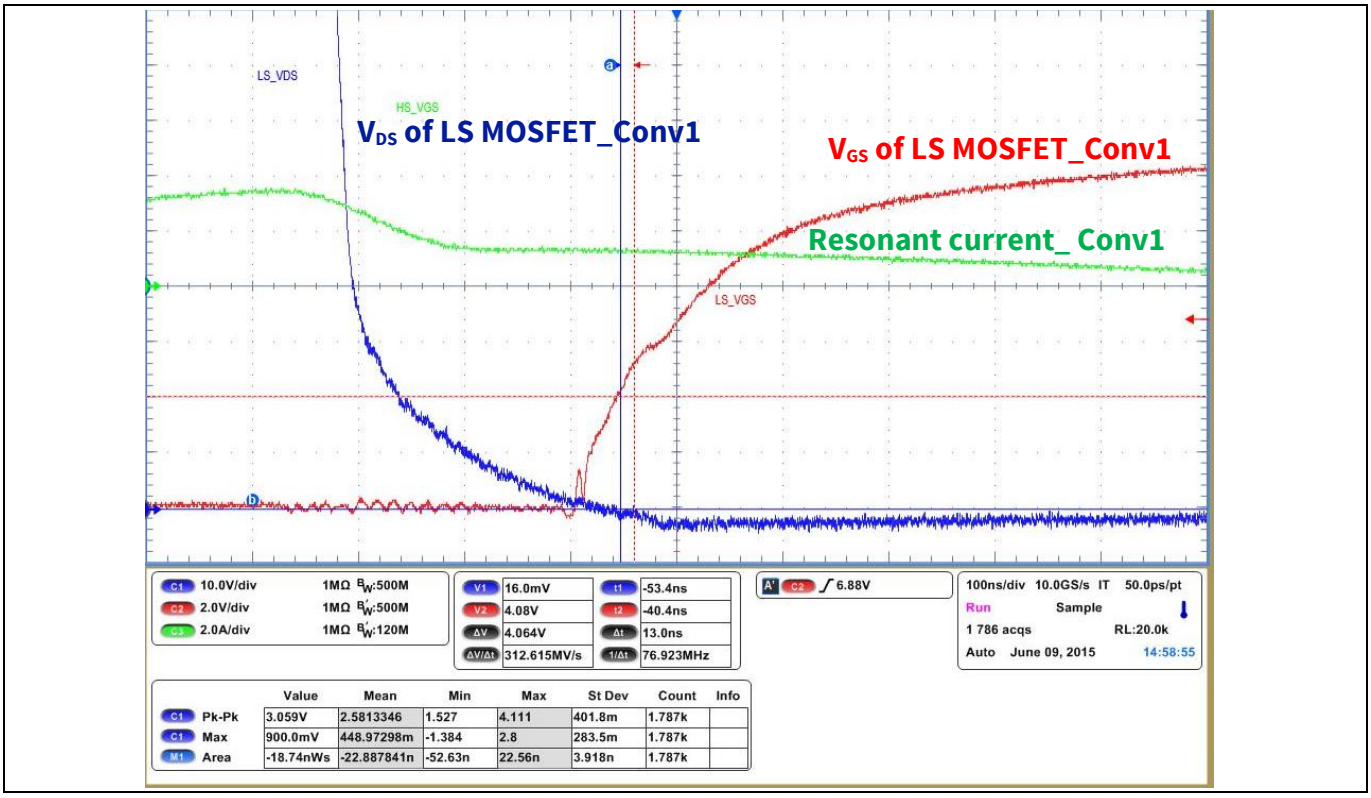



**Figure 39 Full ZVS turn-on at only 3% load (90 W) and $V_{in}$ = 380 V DC (Conv1)**

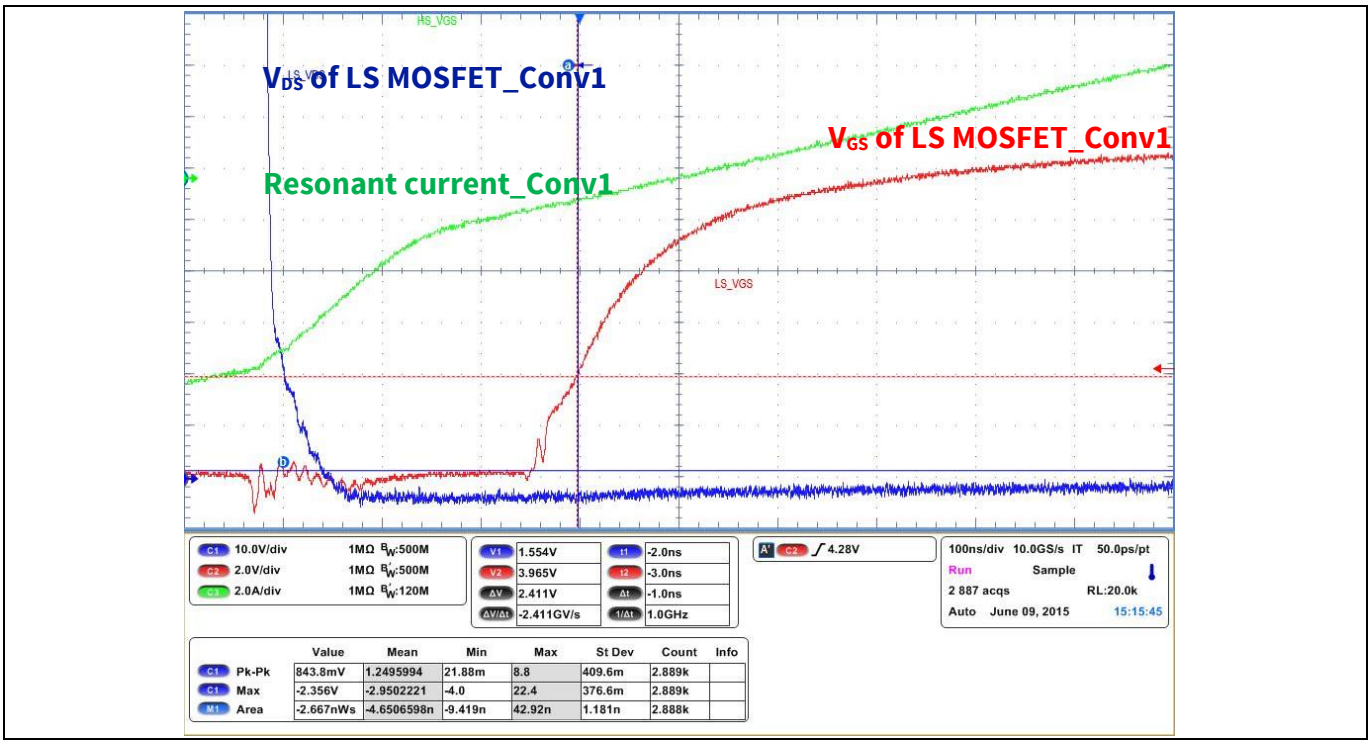



**Figure 40 Full ZVS turn-on at full load (3000 W) and $V_{in}$ = 380 $V_{DC}$ (Conv1)**

Figures 41–42 show SR operation at 10% and 100% load: the $V_{DS}$ reduced peak measured on the SR MOSFET is the result of an accurate layout and transformer construction, but is also linked to the very low $Q_{rr}$ offered by the OptiMOS™ 5 technology.

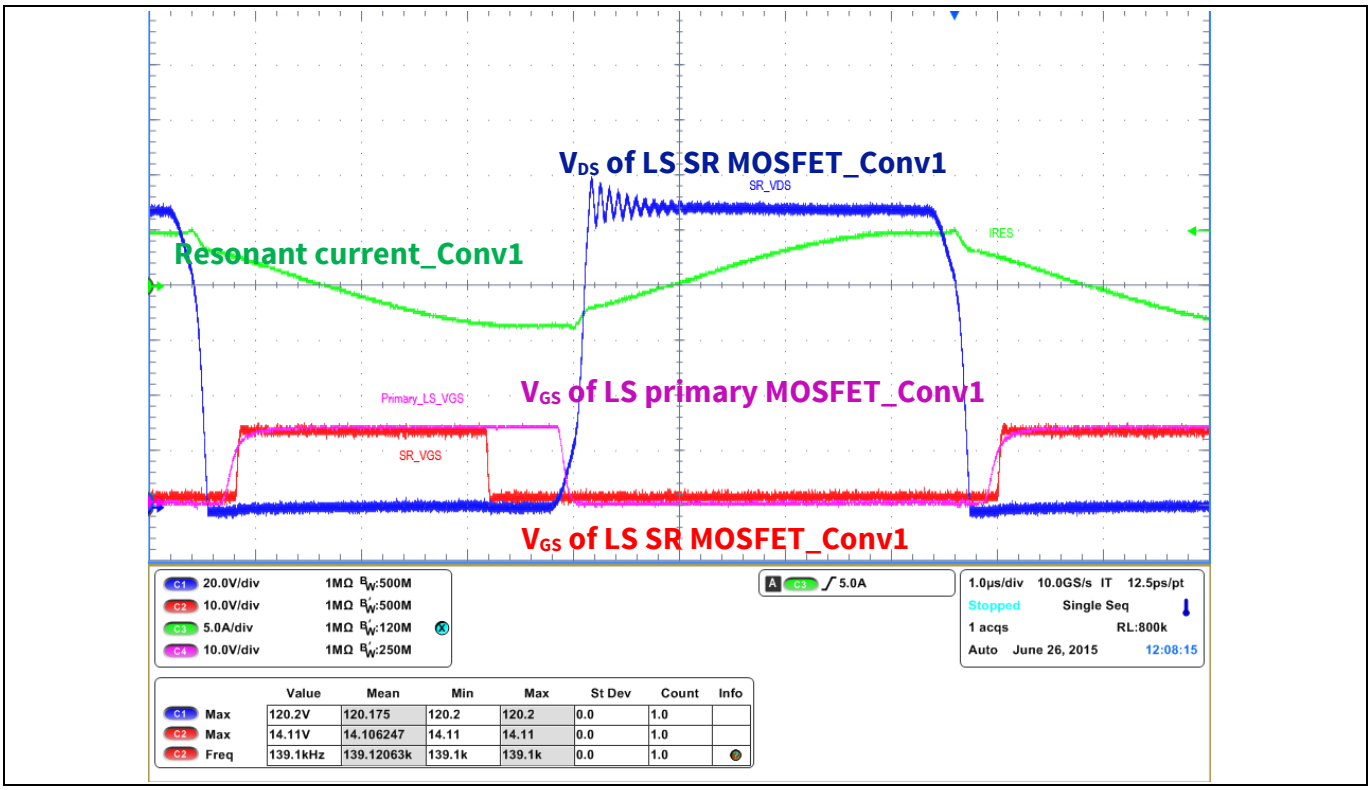



**Figure 41 SR MOSFET operation at 10% load and $V_{in}$ = 380 $V_{DC}$ (Conv1)**

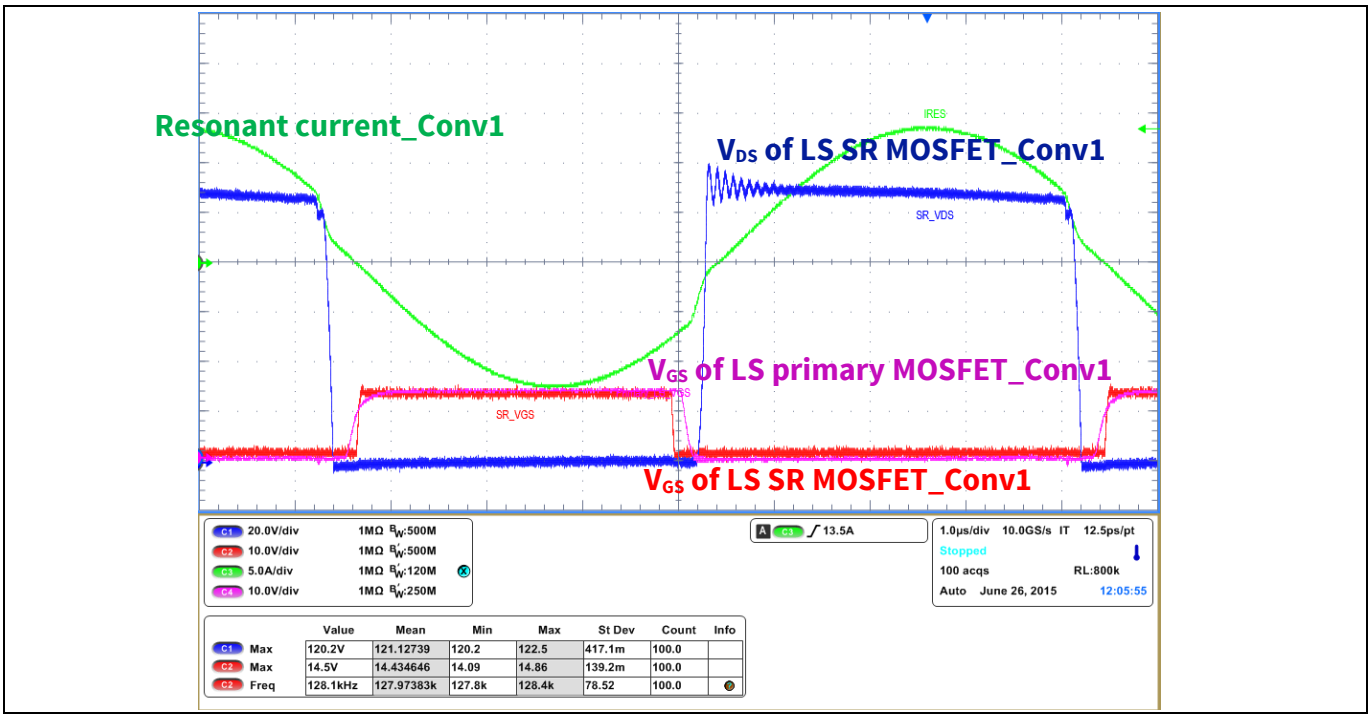



**Figure 42 SR MOSFET operation at full load and $V_{in}$ = 380 $V_{DC}$ (Conv1)**

## 5.2 Efficiency plot

Figure 43 reports the efficiency plot measured on the 3 kW dual-phase LLC assembled with IPW60R031CFD7. The fans and BIAS consumption are not included in the measurement shown.

All measurements have been performed in a fully automated setup and according to the methods described in [13].

A very flat plot can be observed: this is the well-known effect of the phase shedding. Moreover, the efficiency at 100% is not much lower than the 50% load, which gives significant benefits from the thermal perspective.

For the sake of completeness, it should be stated that including BIAS and fan consumption would generate around 3 W additional losses, which would reduce the efficiency by 1% at 10% load, but only 0.1% at full load.

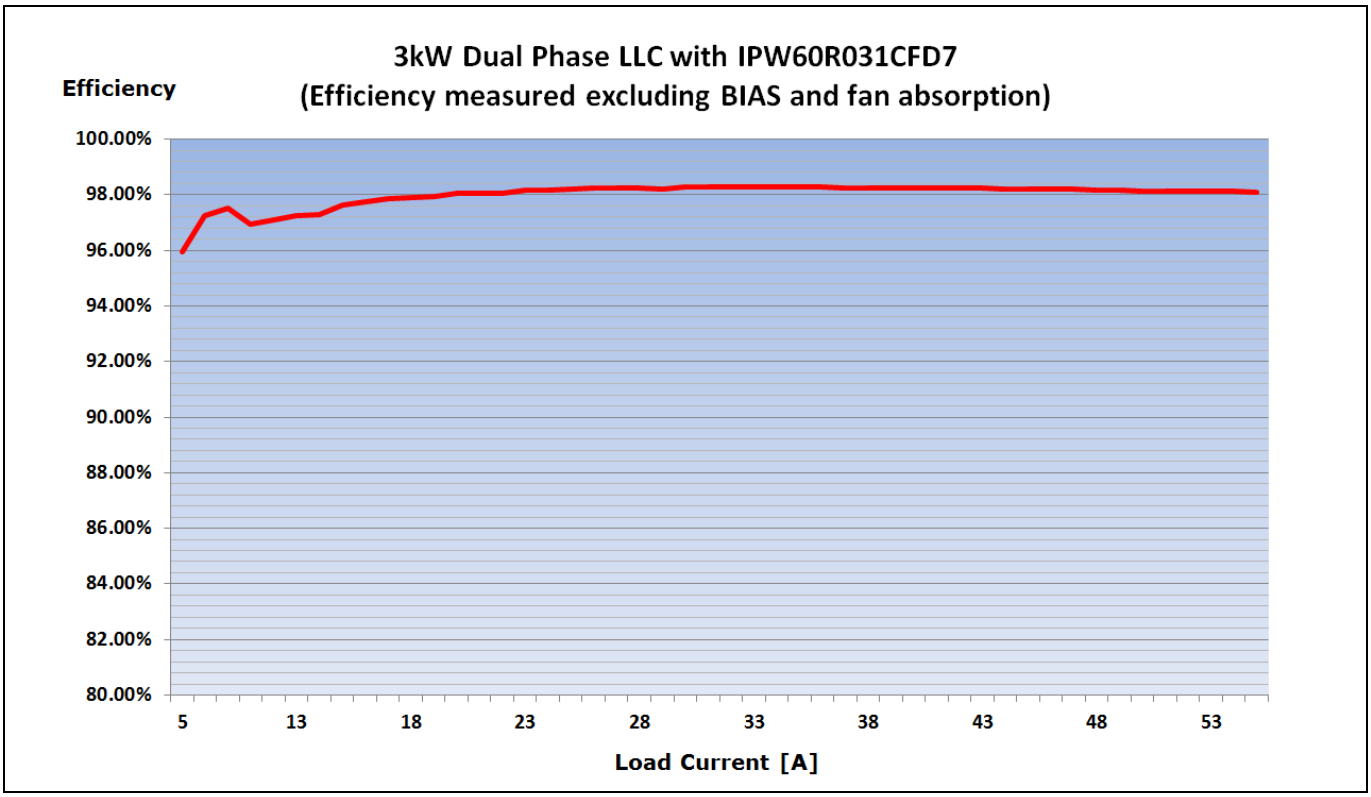



**Figure 43 Efficiency versus load measured with IPW60R031CFD7 at $V_{in}$ = 380 V DC**

The plot above shows that the performance targets set in the technical specification at the beginning have been completely fulfilled.

To highlight the crucial contribution of the 600 V CoolMOS™ CFD7 MOSFET usage in the two HB LLCs, it is worth showing another graph in Figure 44 that includes the Δη measured in the same board in comparison with three competitors' fast body diode devices in a comparable $R_{DS(on)}$ range.

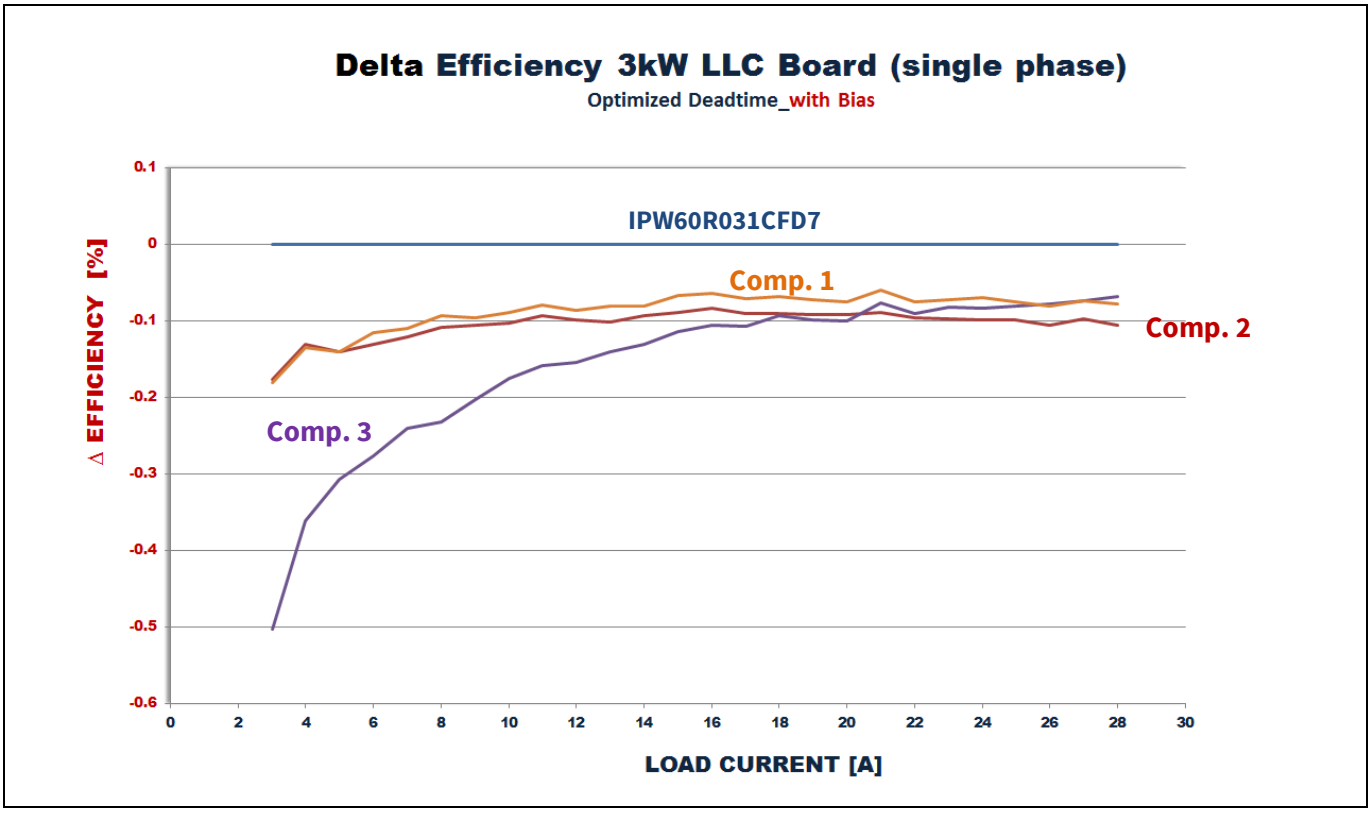



**Figure 44 IPW60R031CFD7 vs three competitors in 3 kW dual-phase LLC**

The plots have been acquired during operation with only one phase activated (1500 W), in order to increase the measurement accuracy, especially at very light load operation. IPW60R031CFD7 is able to achieve better efficiency compared to the three competitors with similar $R_{DS(on)}$ across the entire load range. A significant improvement is visible in the 10–20% load range, up to more than 0.5% vs Competitor 3. This is mainly due to the reduced driving and switching losses, which are dominant in that load range. An improvement is also visible in the 60–100% load range, mostly related to lower typical $R_{DS(on)}$ and switching losses, especially at turn-off.

The analysis of the operation with only one phase activated triggers some interesting considerations about a possible further improvement in the flatness of the efficiency curve.

Figure 45 shows in the same graph both the single phase (Conv1, up to 1500 W, red curve) and the dual-phase efficiency plot (up to 3000 W, blue curve).

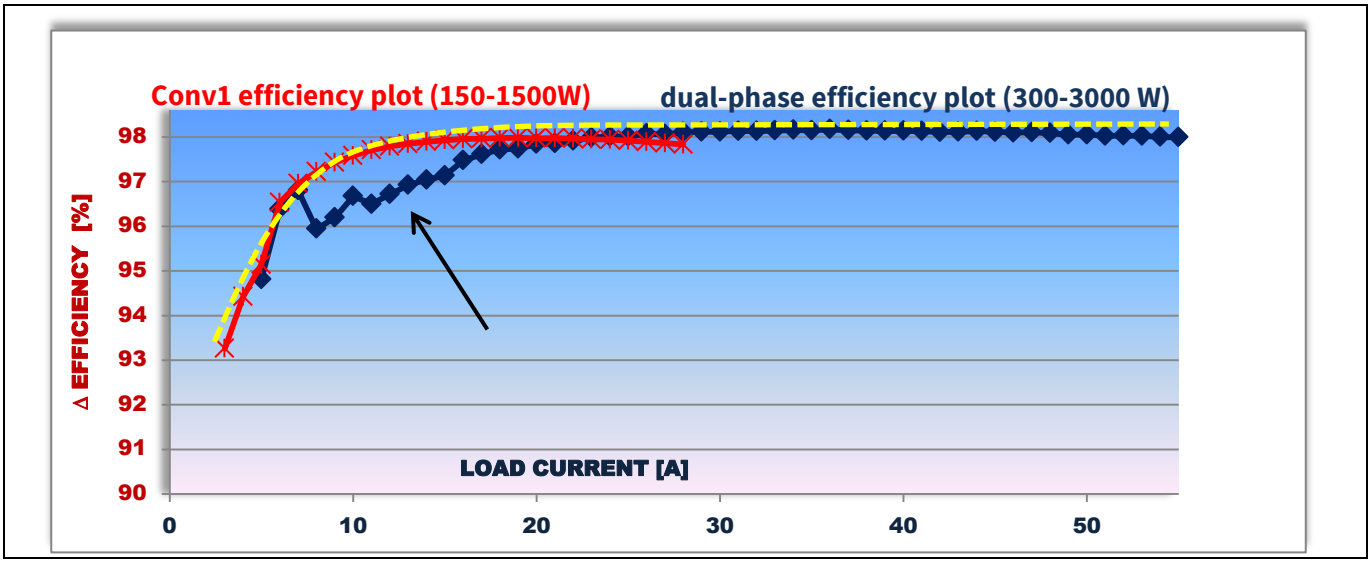



**Figure 45 Single versus dual-phase efficency plot comparison**

The operation of each of the two converters influences the phase shedding, specifically the output current level at which the Conv2 is activated/de-activated. Please refer to the definition of Conv1 and Conv2 as described in Section 4.2 of this document.

In fact the “valley” in the curve highlighted by the arrow in Figure 45 can be explained as follows: by reducing the output load from 100% to 10% load, at the total output current around 15 A, the SR MOSFET of Conv2 switches off, thus inducing the sudden reduction of efficiency in the visible valley. This is due to conduction on the SR MOSFET body diodes.

If the output current is reduced further, below the phase-shedding threshold, the Conv2 switches off and the Conv1 takes over, thus generating the natural sudden increase of efficiency seen in the plot.

We can therefore conclude that a possible way of achieving an even flatter efficiency plot is to switch off the Conv2 while its SR stage is still active. In that way we can minimize the valley described, and get a final curve like the dotted yellow line in Figure 45.

The phase shedding is confirmed to be a very important feature that really shapes the efficiency plot, according to the specific converter’s technical specification requirements.

# 6 Conclusion

The 3 kW dual-phase LLC demo board is the demonstration of how a mix of best-in-class CoolMOS™ and OptiMOS™ power device technologies with proper driver and control ICs enables a power converter design with superior performance and reliability features.

The demo board promotes a full Infineon solution suitable for a multi-phase/interleaving LLC design with phase shedding, by achieving a very high and flat efficiency plot, with the additional benefit of homogeneous heat spreading – necessary conditions to achieve high power density and increase reliability.

The concept enables reliable use of the HB LLC topology, which is the most cost-effective for high-efficiency designs. It demonstrates the good operation of the 600 V CoolMOS™ CFD7, a technology which enables all the benefits of a fast BD device in resonant applications without sacrificing any performance.

The OptiMOS™ 5 150 V series is also shown to have all the necessary features to guarantee efficient and reliable operation in the Synchronous Rectification stage of a complex dual-phase design.

In order to make the board test even more user friendly, a GUI has been designed, enabling engineers to easily interact with the converter during analysis on the bench.

The present document gives an overview of the most relevant design aspects and the considerations behind the decision to build such a demo board.

A Bill of Materials (BOM) and a detailed description of the most important active and passive components used, including the specification of the magnetic parts, are available inside this AN.

Details are also provided about the XMC4400-based digital control features, with an accurate description of the implemented algorithms.

Finally the performances are documented by captured waveforms and efficiency plots: all the results shown have been achieved with the 600 V CoolMOS™ CFD7 in the TO-247 package (IPW60R031CFD7), which results in the most suitable $R_{DS(on)}$ for the analyzed output power range.

# 7 Technical Data Package (TDP)

By clicking on the icon below, the reader can find a file providing a useful summary of all the technical and assembly features of the Infineon 3 kW dual-phase LLC demo board.

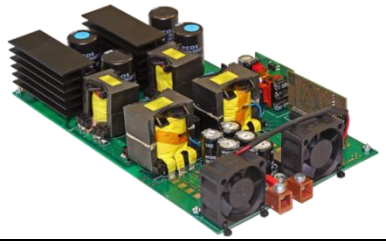


**Figure 46 Technical and assembly features of the Infineon 3 kW dual-phase LLC demo board.**

The BOMs of the motherboard and the two daughter cards are available in this document. The CAD and gerber files are available on request.

A procedure for functional testing is also included: this is exactly the same as that applied to each prototype during mass production.

# 8 Useful materials and links

In the following links, you can find more detailed information about the devices used from Infineon and the magnetic components.

**Primary HV MOSFETs CoolMOS™ IPW60R031CFD7**

www.infineon.com/600v-CFD7

**Microcontroller XMC4400**

*http://www.infineon.com/dgdl/Infineon-XMC4400-DS-v01_01-en.pdf?fileId=db3a30433afc7e3e013b3cfb455565a3*

**Advanced dual-channel gate drive 2EDN7524F**

*http://www.infineon.com/dgdl/Infineon-2EDN752x_2EDN852x-DS-v01_00-EN.pdf?fileId=5546d4624cb7f111014d672f9fbb5142*

**Isolated gate drive 1EDI60N12AF**

*http://www.infineon.com/dgdl/Infineon-1EDI60N12AF-DS-v02_00-EN.pdf?fileId=db3a3043427ac3e201428e5da08f372a*

**Bias QR Flyback controller ICE2QR2280Z**

*http://www.infineon.com/dgdl/Datasheet_ICE2QR2280Z_v21_20110830.pdf?folderId=db3a304412b407950112b408e8c90004&fileId=db3a30432a7fedfc012a8d8038e00473*

**SR MOSFETs OptiMOS™ BSC093N15NS5**

*http://www.infineon.com/dgdl/Infineon-BSC093N15NS5-DS-v02_02-EN.pdf?fileId=5546d462503812bb01507033a3fa1175*

**Main transformer and resonant choke ferrite cores**

*http://en.tdk.eu/blob/519704/download/2/ferrites-and-accessories-data-book-130501.pdf*

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[17] René Mente, “CoolMOS™ 600 V CFD7”, AN_201708_PL52_024, Infineon Technoloigies, 2017

# 10 List of abbreviations

**Table 5**

| Abbreviation | Definition |
|---|---|
| ADC | Analog to Digital Converter |
| BD | Body Diode |
| BOM | Bill of Materials |
| CAD | Computer-Aided Design |
| CCU | Capture and Compare Unit |
| CLT | Coreless Transformer |
| CMTI | Common Mode Transient immunity |
| $C_{OSS}$ | Output Capacitance $C_{OSS} = C_{DS} + C_{GD}$ |
| $C_{o(tr)}$ | Effective output capacitance, time related |
| COM | Communication port |
| $C_r$ | Resonant capacitance |
| CSG | Comparator and Slope Generator |
| DAC | Digital to Analog Converter |
| DC | Direct Current |
| DMA | Direct Memory Access |
| DSP | Digital Signal Proccesor |
| di/dt | Steepness of current slope at turn-off/turn-on |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EMI | Electromagnetic Interference |
| $E_{OSS}$ | Stored energy in output capacitance ($C_{OSS}$) at typ. $V_{DS}$ = 400 V |
| ERU | Event Request Unit |
| FET | Field Effect Transistor |
| FPU | Floating Point Unit |
| $F_{sw}$ | Switching frequency |
| GaN | Gallium nitride |
| GND | Electric ground |
| GUI | Graphical User Interface |
| HB | Half-Bridge |
| HS | High-Side |
| HRC | High Resolution Channel |
| HRPWM | High Resolution PWM |
| HV | High Voltage |
| IC | Integrated Circuit |
| ID | Drain-to-source current |
| IDE | Integrated Development Environment |
| $I_{out_phase}$ | Output current of one converter |

## List of abbreviations

| Abbreviation | Definition |
|---|---|
| $I_{res}$ | Resonant current |
| $I^2C$ | Inter-integrated circuit communication protocol |
| LCD TV | Liquid Crystal Display television |
| $L_r$ | Resonant inductance |
| $L_m$ | Magnetizing inductance |
| LS | Low-Side |
| LV | Low Voltage |
| MAC | Multiplication and Accumulation unit |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NTC | Negative Temperature Coefficient thermistor |
| OCP | Over Current Protection |
| PFC | Power Factor Correction |
| PI | Proportional Integral controller |
| PSU | Power Supply Unit |
| PWM | Pulse Width Modulation |
| $Q_G$ | Gate charge |
| $Q_{OSS}$ | Charge stored in the $C_{OSS}$ |
| QR | Quasi Resonant |
| RAM | Random Access Memory |
| $R_{DS(on)}$ | Drain-source on-state resistance |
| $R_{g,on/off}$ | Gate resistor applied at on and off transitions |
| SMPS | Switched Mode Power Supply |
| SPI | Serial Peripheral Interface |
| SR | Synchronous Rectification |
| SW | Software |
| TDP | Technical Data Package |
| TTL | Transistor-Transistor Logic |
| UART | Universal Asynchronous Receiver-Transmitter |
| USB | Universal Serial Bus |
| USIC | Universal Serial Interface Channel |
| $V_{Bulk}$ | Bulk capacitor voltage |
| $V_{cc}$ | Supply voltage |
| $V_{Cr}$ | Resonant capacitor voltage |
| $V_{DS}$ | Drain-to-source voltage |
| $V_{GS}$ | Gate-to-source voltage |
| $V_{O;PFC}$ | PFC output voltage |
| $V_{out}$ | Output voltage |
| ZVS | Zero Voltage Switching |

# Revision history

### Major changes since the last revision

| Page or reference | Description of change |
|---|---|
| | |
| | |
| | |

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